

G. HAAS

**FUNDAMENTALS AND
COMPONENTS OF
ELECTRONIC DIGITAL
COMPUTERS**

FUNDAMENTALS AND COMPONENTS OF ELECTRONIC DIGITAL COMPUTERS

The technique of electronic digital computers has advanced rapidly in recent years but in the literature published a gap has been left between the advanced treatise and the simple introduction.

Dr. Haas has sought to fill this gap by providing a comprehensive technical introduction to the subject which describes the components and circuits of digital computers and relates them to the tasks they have to perform.

After a short introduction which gives a synopsis of the classification, operation and fields of application of computers, the first part of this book deals with mathematical fundamentals. The principal circuits are then described with the use of block schematic diagrams.

The second part examines the special requirements of individual components, with particular attention paid to static and dynamic properties, whilst the last section gives detailed examples of practical circuits and discusses methods of calculating and dimensioning.

This well illustrated, practical book will provide a sound introduction to a highly important field.

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FUNDAMENTALS AND
COMPONENTS OF ELECTRONIC
DIGITAL COMPUTERS

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DIGITAL COMPUTERS

G. HAAS

1963

P H I L I P S T E C H N I C A L L I B R A R Y

Translated from German by E. Grubba F.I.L. (Eng.), Darmstadt, Germany

Publisher's note:

This book contains xii + 247 pages and 179 illustrations

Other editions in Philips Technical Library in German and French language

U.D.C. 621.389: 681.14

Original German edition:

© N.V. Philips' Gloeilampenfabrieken, Eindhoven, The Netherlands, 1962

English edition:

© N.V. Philips' Gloeilampenfabrieken, Eindhoven, The Netherlands, 1963

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Printed in The Netherlands.

PREFACE

A comprehensive survey of the most important components for electronic digital computers, as well as a description of their use in typical circuits, was given in a number of papers published by the author in laboratory reports. The circuits themselves which, as a rule, can be reduced to a few simple basic circuits, are also of importance in other fields of information technique. It seemed, however, of little purpose to consider the circuits in complete isolation. By investigating the tasks which they fulfil as components in electronic computers, we have gained a picture which is also useful in other fields.

The author has gladly followed the suggestion of the publishers to allow this series of papers to appear as a book. In view of the enormous strides made by digital techniques in but a few years, and anticipating further rapid development, this book cannot in any way claim to be comprehensive; this holds good with respect to the principles as well as to the components and circuits described. The book is merely intended as an introduction to digital computing which will provide the reader with easy access to the actual problems. The literature quoted at the end of the book will be helpful in this respect. With these points in mind, the contents have been limited to the essential fundamentals, and only those components have been included which are already firmly established in the technique of digital information processing.

The contents of the book are chiefly based on the publications mentioned above, though some rearrangements and enlargements have been made. Apart from the introduction, the book is divided into three main parts: The part, "Fundamentals of electronic digital computers" deals first with the various numeral systems and discusses the mathematical fundamentals of electronic computing. Then follows a schematic description of those circuits which in part carry out logical combinations and in part act as switches or sources of static voltages. They also make up most of the circuits used in computers. After dealing with the different methods of storing, there finally follow examples in block circuit diagram form of some binary and decimal arithmetic units. The section "Components" deals with the special problems of the individual elements, the vacuum tubes, cold cathode tubes, semiconductor diodes, transistors and magnetic cores with rectangular hysteresis

loop. At the same time, attention is paid to the static and dynamic properties and stress is laid on those aspects which are important for use in computers and which contribute to the understanding of the information contained in the technical data sheets, without going into further details concerning the physical fundamentals and exact data. The last section deals with circuit examples. The most important calculations and hints on dimensioning are given for logical circuits, bistable and monostable flip-flop circuits, decade counters, stores and registers.

The author wishes to express his gratitude to all who have cooperated by valuable advice in the making of this book, in particular to Mr. W. Sparbier, Mr. K. Wagner and Dr. F. Weitzsch.

December, 1962

The Author

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CHAPTER 1

INTRODUCTION

Science, technology and administration have to cope with an increasing number of mathematical problems which cannot be solved satisfactorily, or only with great difficulty, by ordinary office calculating machines, considering the expense involved in time and labour. There are physical and technological problems whose solution is beyond the scope of mechanical calculators. Moreover, there are tasks which carry certain commercial or technical advantages when speedily tackled, as for instance in the calculation of tenders, in production control, when undertaking current experiments or executing orders with a fixed delivery date, etc. The progress of automation in production [1] and in the compiling of data for office and administrative work, frequently demands the employment of automatic computers [2, 3], so that in the field of calculating machines, the transition from ordinary office calculator to automatic computer corresponds to the progress from mechanisation to automation.

Apart from the obvious use in predominantly calculating work, the digital electronic computer technique has achieved great importance in several other fields where information is compiled. This technique was therefore introduced in digital control and regulating systems [70], where, for example, the centre of the control unit is a computer which supplies the manipulated variable from the controlled condition. Such systems are more accurate and often more flexible than those using analogue circuits. Electronic telephone exchange techniques providing the desired connections rely on the computer system [80].

1.1 Classification of electronic computers

Computers can be classified in various ways such as nature and extent of problems to be solved, arithmetic speed, method of figure presentation or manipulation. We propose to start with the chart in Fig. 1.1. from which it should be noted that at times there are no definite distinctions between the different systems.

The hand- or motor-operated mechanical office calculators [4] can add

and subtract (accounting machines, adding machines, cash registers) or add, subtract and multiply (e.g. invoicing machines) or perform all four basic arithmetical functions (calculators). The arithmetical speed of these machines is considerably increased if an electronic mechanism is substituted for the mechanical register. Since mechanical multiplication in particular is relatively slow, there is a growing use of electronic multiplication as far as office calculating machinery is concerned, while adding and subtracting are often still being done mechanically. Human labour, however, is indispensable for that type of calculating machine in processing intermediate results and manipulating new sets of figures and calculations.

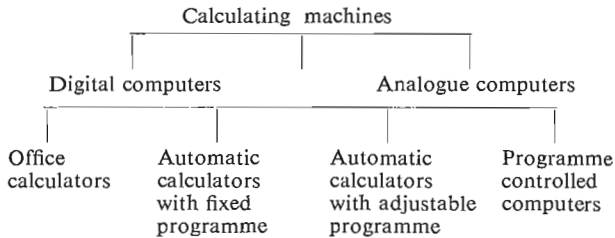


Fig. 1.1 Classification of calculating machines

In order to make full use of the immense arithmetical speed of the electronic register, human interference in the various calculating stages must be avoided as far as possible and should be replaced by the machine itself. The first step in that direction is the combination of office calculators with typewriters, tabulating machines, card-punching machines, indexing machines etc. into automatic calculators with fixed programme, thereby achieving a very high degree of mechanisation in office work. Such machines are capable of performing certain arithmetical operations automatically; these operations, however, are confined to a certain process in each case; their programme is fixed. Electronic registers in conjunction with mechanically operating card-punching machines (Remington Rand) or electromagnetic machines (IBM, Bull) also have the advantage that they operate speedily in comparison with mechanical operations such as the sorting of cards, so that the extra work they produce requires no extra time. Card-punching machines with electronic accessories are employed with advantage wherever a lot of figures must be compiled and processed in accordance with continuously recurring rules, e.g. in book-keeping where accounts are made up and booked automatically, in bank accounting, in store-keeping, for wages accounting, etc. (single purpose machines).

A further step in the perfecting of electronic computers lies in the fact that not only certain fixed calculations but a wide choice of varied calculations can be carried out. There are two ways of achieving this: The calculating scheme can be arranged on a switchboard by appropriate connections between the respective circuits, thus obtaining an automatic calculator with adjustable programme which executes a complete computer programme automatically according to the circuit chosen with a limited number of single operations. With appropriate programming on the switchboard, machines of this type can be employed for the most varied technical and commercial purposes. Their somewhat rigid method of operation, however, cannot cope with all the problems. An all-purpose machine is only obtained if each instruction of the computer programme is given exactly as the calculation figures in code, either by feeding the instructions one after the other into the machine during the calculation process (on punched cards, punched tape or magnetic tape) or by storing them before the calculation process begins in a storage device. These programme controlled computers are thus capable of solving the most varied mathematical problems with automatic operation and control in a long series of calculations step by step according to a fixed programme. They are also capable of making use of the information obtained in the calculating process and of making certain decisions by repeating certain fixed arithmetical steps governed by the character of an intermediate result, or by making a choice between several possible ways.

In the calculating machines mentioned so far, the figures are produced by a discontinuous digital series, e.g. in mechanical office calculators by ten marked settings of the counting wheels. We speak therefore, of *digital computers*. The figures, however, can also be produced by a physical quantity such as length, angle of rotation, voltage, etc. In that case we talk of *analogue computers* because the arithmetical problem is then solved with the aid of physical processes which are analogous to the problem; in other words they are governed by the same principles. The result is registered as a pointer setting on a measuring instrument, on paper as a graph, or, with the repeating analogue computers, appears on the tube of an oscillograph. To this category belong, for instance, the integrating instruments and, as the most elementary example, the slide rule. Analogue computers can be constructed on a mechanical, electromechanical or electronic basis, and frequently serve to solve common differential equations in mathematics and technology or as a building stone in regulator and control techniques.

1.2 Synopsis of electronic computing

To ensure reliable service we employ the components used in digital com-

puters in only two phases of operation, the most extreme ones possible, e.g. when the device (triode or transistor) is "open" (conducting) and when it is blocked. This means, on the other hand, that we are forced to express all information (figures and instructions) which the computer is to process by a combination of two kinds of values.

It seems reasonable then, to employ in computers the binary number system with its two digits 0 and L *).

When static, (e.g. during storage) the two digits are represented by two potentials of different values; in dynamic representation (e.g. in line transmission) by the presence or absence of pulses in certain places.

The actual arithmetical operation takes place in the arithmetical unit which is capable of adding binary numbers according to the basic rules of arithmetic. Apart from adding up, the arithmetical unit must be capable of two further operations: Complement production and index value transposition. By producing a complementary function, subtraction is reduced to addition by converting the subtrahend, through adding a constant, into a positive value whose addition to the minuend (omitting the highest numeral) produces the differential. The transposition of the index value by means of a shift register makes it possible to convert the multiplication process into a continuous addition and division into continuous subtraction. All arithmetical problems beyond the scope of the four fundamental rules of arithmetic must be converted to these rules by suitable programming. As a rule, the number of stages in this case is unimportant in view of the great arithmetical speed.

The binary system requires the conversion from or into the decimal system at the input and output of the machine. To avoid an elaborate and expensive operation necessary for this operation, other numerical systems are frequently used, as, for example, the binary coded where only the individual numerals and not the complete decimal are converted each time into binary numbers in accordance with a specific rule. Here too, the arithmetical unit is capable of binary calculations for which, however, certain additional corrections are necessary. Furthermore, it is also possible to work directly in the decimal system. Since the computer disposes only of binary data, however, a direct arithmetical combination as in the binary system is not possible in this case; we have to go back here to the method of counting pulses. The arithmetical unit thus consists mainly of counting circuits which, in turn, are composed of bistable elements. Finally, electronic computing can be carried out with the aid of translators [81]. For multiplication in the decimal system, for instance, we use a multiplication table unit consisting

*) We have chosen the letter L in this case to avoid any confusion with the decimal "1".

of a matrix with 10 horizontal and 10 vertical inputs covering the units 0 to 9. A pulse on both line 3 and column 5, for example, through coincidence at the point of junction thus produces a pulse coordinated with the product 15.

The circuits used in computers can be made up from a few fundamental circuits. The binary connections and the numerous functions in circuit and combination systems are carried out by so-called logical circuits whereas storing and counting are done with the aid of bistable flip-flop connections. Fundamental circuits can be built up with thermionic tubes, gasfilled tubes, transistors, transfluxors and in part with semiconductor diodes. The criteria as to the suitability of a component are, above all, its reliability, switching speed, size and heat development.

1.3 Synopsis of the main parts in a programme controlled computer and their coordination

Let us first discuss briefly the functions of a programme controlled computer. It is the most advanced stage in the development of calculating machines and generally contains all the main parts which are only partially found in simpler electronic computers or other systems for processing information.

The decisive progress modern computers have made over earlier calculating machines is in programme control. A programme controlled computer is capable of carrying out long series of arithmetical operations based on a freely selective computer plan fed into the machine. It is also capable of making use of the information obtained in the course of the calculation and of making certain decisions on its own.

The main parts of a programme controlled computer are shown in the diagram of Fig. 1.2:

The *input* takes in the information consisting of the figures and computing instructions in the form intelligible to the machine. The instructions and figures, generally called "words", are fed into the input, on punched cards, punched tape or magnetic tape for instance, where the recorded information is scanned (mechanically, optically or magnetically), converted into electronic pulses and passed on via the information line I_1 to the storage unit. Since the conversion of the scanned information into electric pulses takes place at far greater speed than the feeding in of the information, the input is equipped with a storage device (buffer) to accumulate a certain amount of information. Furthermore, the input must have circuits which code the decimal system appropriately (e.g. in the binary representation). The figures are reproduced as a series of electric pulses. In that case a particular digit is

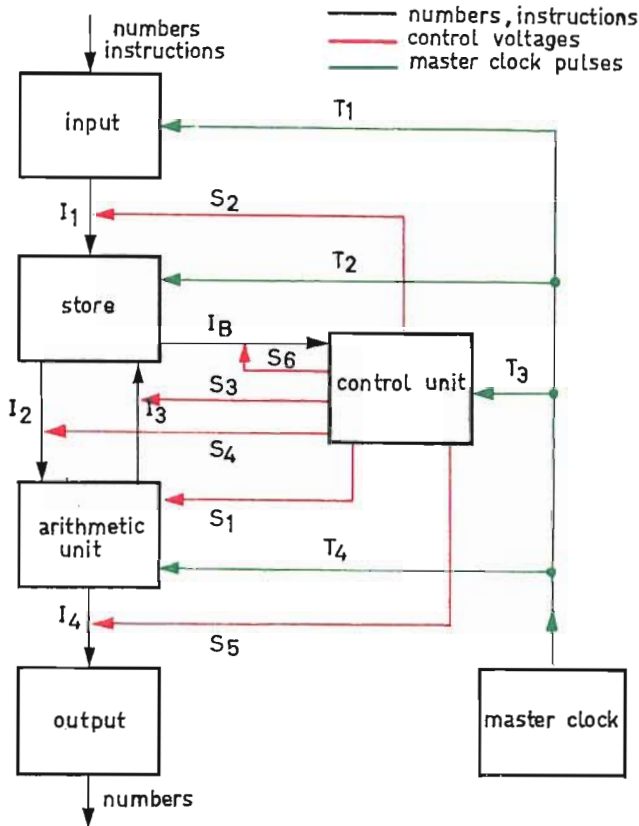


Fig. 1.2 Block circuit diagram of a programme-controlled computer

represented not by the strength of a pulse but according to a certain code by the presence or absence of pulses at certain points; in other words, by appropriate combinations of positive — negative values or by a definite number of pulses.

The reverse process operates in the *output*. The result calculated inside the machine is made available to the outside by being recorded on punched or magnetic tape, or by being printed by an electric typewriter.

The new figures made up from the numbers fed in according to the rules of the basic arithmetical operations are produced in the *arithmetic unit*. Basically it achieves no more than a calculator; that is to say, it is usually capable of adding, subtracting, multiplying and dividing two figures. In addition to the adding circuit it contains the so-called registers in which the operands are stored during the arithmetical operation. These operands are

fed into the arithmetical unit via line I_2 , if not already in the register. The result either remains in the register (accumulator) or is passed via I_3 to the storage unit or via I_4 directly to the output.

The *storage unit* serves to store the figures as well as the initial values of the problem, the intermediate results and frequently also the computing instructions. It is the depository of all data important to the machine and holds this information in readiness for a call. Storing is done binary, i.e. in the form of positive-negative values. The capacity of up-to-date programme-controlled machines lies approximately between 50 and 20,000 decimals of ten places. The space inside the storage unit set aside for storing a word is called a storage cell. The cells have consecutive numbers which give their "addresses" so to speak. For practical purposes the storage unit is generally sub-divided into several compartments of different functions and construction. In addition constant registers are often built in; these are storage units for numerical values which are frequently used ($\frac{1}{2}$, e , π , etc.) from which readings only can be taken. Apart from these "internal storage units", the calculators often also have external storage possibilities such as punched tape, magnetic tape or discs. These relieve the main storage unit and serve to accumulate information rarely required or only needed at a later time. In principle the storage units fulfil the following three tasks:

1. Accumulation of information not supplied simultaneously so that a link-up is possible. Thus, for example, the sequence of instructions is fed into the machine before computing; the figures to which it is to be applied, however, are produced only during the course of the computing process.
2. Accumulation of intermediate results in order to carry out an operation in stages (e.g. multiplication) in the arithmetical unit. A method of operation in the arithmetical unit without the aid of a storage unit would be possible in principle, but would require an enormous amount of switching equipment.
3. Storing the computed result until it can be made available for external use (e.g. during reading time).

The *control unit* coordinates the functions between the other components of the machine. It obtains via I_B the instructions step by step from the storage unit, while during this process each instruction is stored in the register of the control unit. The so-called decoding circuits are connected with the register; they convert the information contained in the instructions (addresses of storage cells and arithmetical operations) into the corresponding control voltages. The register is set to the required arithmetical operation via

the control line S_1 ; by operating the appropriate switches the control signals across the lines S_2 , S_3 , S_4 and S_5 regulate the necessary numerical traffic between input and store, store and arithmetical unit and arithmetical unit and output as indicated by the arrows in the corresponding information lines. The control voltage of control line S_6 finally provides that after completion of one arithmetical stage the next instruction is supplied to the control unit via I_B .

The *master clock* is a pulse generator which times the entire machine and produces the pulses necessary for the electrical representation of the figures. Via the line T_1 the input receives a periodic pulse sequence from which the electrical representation of the figures is obtained. The lines T_2 , T_3 and T_4 effect the synchronous operation of the processes in the store, the control unit and the arithmetic unit. The pulse series frequency of the clock lies between 20 kc/s and 5 Mc/s with up-to-date computers.

Each instruction reaching the control unit means a new step in the progress of the computer programme, consisting of the switch- and operation phase. During the switch phase the connections needed for this arithmetical step are made and the arithmetical unit is adjusted to the desired arithmetical operation. The actual computation then takes place during the operation phase in the arithmetic unit. In very simple terms, the functions of a computer during an arithmetical stage are something like this: The instruction is fed into the control unit and stored. Here it causes one figure from a particular storage cell to be transmitted to the arithmetical unit where it stays in store until a second figure reaches the arithmetical unit whereupon both are, for example, multiplied; finally the instruction sends the result to the output where it remains in store for the period required to print it. A new stage can commence automatically after a certain lapse of time (synchronous computers) or each time after completion of the preceding step through releasing a special signal (asynchronous computers).

The transfer and conversion of the information inside the machine in the shape of electric pulses can be carried out in two ways: The individual digits of the figures or coded instructions are either transmitted across a line in periodic succession or each digit has its own line and the transmission of all digits is done simultaneously. We call the first case a series computer and the second a parallel computer. It will be obvious at once that the amount of switching equipment for the register is greater in a parallel machine since here a separate adding device must be available for each digit. The control unit, however, is simpler in this case than in a series machine and the arithmetical speed will be higher as a rule.

Computers vary considerably with regard to *arithmetical speed*. The

speed is determined in the first place by the frequency of the master clock which has a top limit on account of the resolution speed limit of the switching equipment employed. With a given clock frequency the arithmetical speed depends above all on the numerical system chosen, on the method of processing the figures (in series or in parallel), on the storage system used, on the addressing and on the operation plan of the machine. With a 40-digit binary series machine (about 12 decimal places) of 100 kc/s clock frequency we require about 1 ms for an addition including all necessary control operations. A multiplication takes about 4 ms. A machine of this type requires about five hours to solve 80 simultaneous operations (the amount of expenditure to solve simultaneous equation systems increases with the cubic number of the equation). An ordinary office calculator would take several months to accomplish this task. Recently designed computers, for instance, are capable of multiplying to 13 places of decimals in 30 μ sec. The speed with which the purely arithmetical operation is carried out, however, is not sufficient to provide a speedy computer on the whole. For this purpose the input and output of the figures, as well as the storage, must be adapted to the speed of the arithmetical unit. Modern developments therefore tend to synchronise the operation times of the individual main parts. In theory the arithmetical speed limit is governed by the speed limit of the pulse transmission along the connecting lines in the machine.

THE FUNDAMENTALS OF ELECTRONIC DIGITAL COMPUTERS

2.1 The solution of mathematical problems

In solving mathematical problems with a programme controlled computer, the automatic computation is only one part of the work required. Altogether we must distinguish between the following successive operations: The finding of a numerical system suitable for the machine, the production of the programme, the setting of the programme and the digits, the automatic computation and the presentation of the results.

2.1.1 NUMERICAL SYSTEMS FOR DIGITAL COMPUTERS [5, 6]

Although the calculator as a rule is only capable of working with the four fundamental rules of arithmetic, electronic computers can in principle cope with all numerical problems whose solution can be divided into a finite number of steps which, in turn, consist only of fundamental arithmetical operations (problems soluble arithmetically). If the problem cannot be solved with the fundamental rules of arithmetic right from the start, as for example, with the solution of a system of linear equations or with most commercial calculating work, then it is a task for applied mathematics to reduce the problem (e.g. the determination of roots of polynomials of the n th degree or the solving of common differential equations) to the fundamental rules of arithmetic. In practical analysis a number of such systems has been known for some time. Whereas for numerical approximations one once looked for smoothly operating systems which achieve their aim in a few steps — whereby the small number of steps was paid for by their complexity — computers require the simplest methods possible which can consist of practically any number of steps. A power series converging only after several hundred steps is more suitable for the computer than an approximation depending on complicated polynomials which might supply a satisfactory solution after one or two steps. In general it can be said that when solving mathematical problems by means of computers the direct approach to the problem is better than substitute or reproduction methods. Especially suitable for fast computers are methods of solving problems in which the same groups of formulae are repeated as often as possible — where-

by only the figures to be inserted are changed (iterative and repetitive methods). The arithmetical operations are thus the same with every step so that instructions into the machine need only be given for one step. In that case we talk of cyclic operations which are desirable for all frequently recurring functions whose calculation exceeds the scope of the four fundamental arithmetical operations. As straightforward examples we shall now deal with the solution of polynomials and the extraction of roots.

In order to determine the functional value of the whole rational function (polynomial of the n th degree)

$$f(x) = a_0 + a_1x + a_2x^2 + \dots + a_nx^n$$

we split up $f(x)$ in continuous division by x into:

$$\begin{aligned} f(x) &= x f_1(x) + a_0 \\ f_1(x) &= x f_2(x) + a_1 \\ &\vdots \quad \quad \quad \vdots \quad \quad \quad \vdots \\ f_{n-1}(x) &= x f_n(x) + a_{n-1} \\ f_n(x) &= a_n \end{aligned}$$

Thus the problem has been reduced to the fundamentals of arithmetic and has become cyclic because for programming we now need merely feed into the machine the relation

$$f_k(x) = x f_{k+1}(x) + a_k$$

and let the calculation begin with $f_n(x) = a_n$, providing the correct constant a_k is extracted from the storage unit for every step. For that purpose the constants a_0 to a_n are arranged in consecutive storage cell numbers and the storage address is reduced by 1 after every step. The sequence of instructions then runs:

1. Multiply the figure f_{k+1} in the arithmetic unit by x
2. Store the result $x f_{k+1}$ in the arithmetic unit
3. Extract from storage cell the constant a_k and add to $x f_{k+1}$.
4. Store the total $x f_{k+1} + a_k = f_k$ in the arithmetic unit.

With this method we calculate, for instance, the function $\log x$, $\cos x$, $\arctan x$, etc.

When *extracting the root*

$$y = \sqrt{x}$$

we can obtain the functional value according to Newton's Law as zero

digits of corresponding polynomials by employing the fundamentals of arithmetic. By squaring we obtain, for example, the polynomial

$$f(y) = y^2 - x = 0$$

whose n th approximation has the form:

$$y_n = \frac{1}{2} \left(y_{n-1} + \frac{x}{y_{n-1}} \right)$$

In executing this instruction step by step with the aid of the y_{n-1} obtained each time through the preceding step, we achieve after a definite number of steps the root value with the required degree of accuracy.

In exactly the same way we obtain for the step-by-step solution of the function

$$y = 1/\sqrt{x}$$

the cyclic relation

$$y_n = y_{n-1} \left(\frac{2}{3} - \frac{x y_{n-1}^2}{2} \right)$$

Such cyclic instructions can be planned in the machine as fixed sub-routine programmes. Thus, if at one point of the programme a functional value is required by means of the cyclic method, the machine switches over to the corresponding sub-routine programme through an appropriate jump instruction (see Section 2.1.4) which takes over the calculating process.

2.1.2 PROGRAMMING [82, 83]

Having found a suitable numerical system for the problem in hand we now proceed with the programming by dividing up the formulae into simple arithmetical operations and introducing the logical operations which make up for the lack of power of decision in the machine. The arithmetical and logical operations constitute the calculating instructions which together make up the computer programme. Programming corresponds to an explicit description of the numerical solution of the problem which would make it possible for the calculation to be carried out by a person possessing no knowledge except the fundamental rules of arithmetic and a certain capacity for discrimination.

The computer programme must subsequently be shaped in a way comprehensible to the machine. For that purpose the appropriate instruction is recorded in code on punched or magnetic tape for each step of the calculation, or a suitable programme routing is carried out. The series of instruc-

tions appertaining to the problem is thus obtained. This is the computer programme for the solution of the problem translated into the language of the machine.

2.1.3 INSTRUCTION SYSTEMS

With machines which store the instructions, the series of data is fed into the storage unit via the input. Here, in general, the separate instructions are kept in consecutive cells; under the term cell we understand the place marked by an index figure (the address) for the intake of a word into the storage unit.

When the machine is switched on, the instructions are extracted step by step from the storage unit and appropriately guided through the computing process by the control unit. As in the case of numbers, the use of binary figures is obvious for the presentation of the instructions. Then the cells of the storage unit can be filled with figures or instructions as required. We distinguish between several methods of giving the instructions.

With the *single address code* each instruction contains only two items of information. The first part of the pulse sequence representing this instruction contains the address of the operand necessary for the operation, the second the method of computing. The information for the calculation ensures that the operand is correctly handled in the arithmetic unit while that of the address allows the number required in the computation to be extracted from the storage unit. Thus three instructions are usually necessary for one arithmetical step, e.g. for the multiplication $A \times B = C$.

Instruction 1: Take reading A from cell x.

Instruction 2: Take reading B from cell y and multiply by x.

Instruction 3: Store C in cell z.

If one operand is already stored in the arithmetic unit as an intermediate result, or if the new solution is to stay in the arithmetic unit, only two or one instructions per arithmetical step will suffice. Since the single address code contains no information about the address of the next instruction, the data in such machines must be assembled in the storage unit in a definite order so that after accomplishment of the n th instruction, the $(n + 1)$ th instruction can be carried out. This has the drawback that there is no freedom in filling up the storage unit.

With some machines up to four addresses are frequently given with each instruction, two for each operand, the address of the result and the address of the next instruction. With three-address machines the address of the

succeeding instruction is missing. A four-address code, for example, looks as follows:

62 3 12 08 51

It signifies that: "The figure from storage cell 62 is to be multiplied ('3' taken as the symbol for multiplication) by the figure from storage cell 12 and the product is to be stored in cell 08. The next instruction is to be read from storage cell 51." With the information of the address of the succeeding instruction we are here no longer tied to a prescribed order as regards the input in the storage unit so that there is greater freedom for programming. Furthermore, we have the advantage of an economy in instructions; on the other hand, unnecessary space will be used in arithmetical steps which only need one or two addresses.

2.1.4 JUMP INSTRUCTIONS [7]

In general, the calculation instructions are recorded in the order in which they are later to be carried out by the machine. If a section from a calculating programme is to be repeated cyclically, that is to say, if a definite group of instructions is to be carried out several times consecutively, then a special instruction must be provided at the conclusion of the last step in the cycle so that the machine returns to the first step of the cycle instead of proceeding further in the series of instructions.

If the cycle commences at instruction A_n and extends to instruction A_{n+m} a further instruction A_{n+m+1} , "back to A_n " must follow. Such an instruction is known as an unconditional jump instruction. The machine, however, must also have the capacity to leave a jump instruction cycle so initiated and go over to the next instruction. This is done through the conditional jump instruction A_{n+m+1} which may run: Back to A_n while the computed figure is positive, otherwise go on to instruction A_{n+m+2} . Here the progress of the calculation is governed by a critical value. The figure z in the repetition of the cycle may be known beforehand (for example, number of steps in the approximate solution of differential equations), or is produced first in the progress of the computation through the desired accuracy (e.g. in the extraction of roots). In the first case, after the last instruction of the cycle we have the instruction A_{n+m+1} : "decrease z by 1, back to A_n , as long as $z > 0$, then to A_{n+m+2} ". In the other case we allow for a certain tolerance δ in the machine, and after the instruction A_{n+m} , through a further instruction, the difference between δ and the difference of two consecutive computed functional values is formed:

$$|y_k - y_{k+1}| - \delta$$

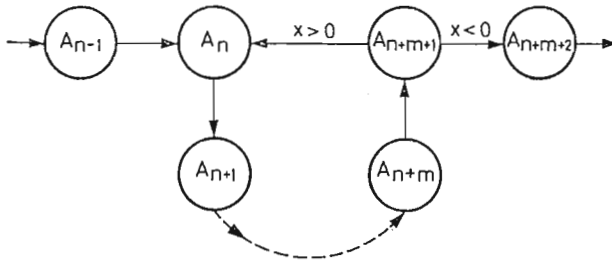


Fig. 2.1 Cyclic section of an instruction series

The cycle is interrupted if this difference becomes negative, that is when the difference between the consecutive steps is less than the given value δ .

Differentiation can also be made in like manner with the help of jump instructions, e.g. through the instruction: "If $y > 0$, then go on to instruction A_k , if $y < 0$, go to instruction A_{k+1} ."

In the computation in which the instruction series are disposed according to the way they will run, cyclic sectional problems appear as a continuous loop. Fig. 2.1 shows an example where through the calculated amount, the instruction A_{n+m+1} decides whether the cycle is to be repeated or the next instruction A_{n+m+2} is to be carried out.

2.1.5 COMPUTING ADDRESSES WITH THE MACHINE

An important property of the programme controlled computer is its ability to work with addresses which were ascertained by the machine itself during the calculation process. For example, in a cyclic process in which other constants are necessary for each cycle (e.g. $1/n!$) the necessary constants must be provided within the cycle for changing the address for the next step. This causes no difficulties with machines in which instructions are deposited in the storage unit, since in this case computation is possible with the instructions as with figures. With machines controlled by punched tape, however, the instructions cannot be altered within a cycle. Here a small intermediate storage unit called the *i*-register [7] is of assistance. This registers the new computed address and the punched tape itself only contains the general instruction to collect the missing address from the *i*-register. This process has the advantage of greater certainty in computing since otherwise an error in calculating with instructions would have far-reaching consequences.

2.1.6 COMPUTING ACCURACY

The accuracy of a computer is determined with a given index figure by the errors in approximation and breaking off. In order to operate with a fixed index figure in the machine, electronic computers with a fixed decimal point calculate with proper fractions of this index figure (all figures transformed into the range $-1 < x < +1$). There is no place for digits added later in the computation, especially in multiplication and division, and the results are falsified in consequence. By means of suitable approximations we take pains to keep the mistakes small; the approximation adjustment must be symmetrical so that the mean error disappears.

The breakdown error frequently occurs where an indefinite number of steps would be necessary to reach true values and the calculation is broken off after a limited number of steps (for instance, in cyclic processes). It decreases with a rising number of arithmetical steps; otherwise the approximation error gains in significance from step to step. In order to keep accumulated errors to a minimum in the solution of a problem, the number of steps to be carried out by the machine must be precisely calculated.

2.2 The numerical systems [5, 7, 8]

The representation of a number by digits forms the basic key to a specific numeral system. In a numeral system of the base B , the complete figure x of N places can be represented by

$$x = \sum_0^{N-1} x_n B^n \quad (2.1)$$

The x_n are the digits of the number x and lie between 0 and B ($0 \leq x_n < B$). The ordinary decimal system is the exception with $B = 10$. In order to make it possible to represent differing figures B must be ≥ 2 . On the other hand, in a numerical system with the base B we also need different B digits ($0, 1, 2, \dots, B-1$). In electronic computers we mainly use the binary number system, the decimal system and the so-called binary coded decimal system. Each of these systems has advantages and disadvantages with respect to the conversion from or into the decimal system, the cost of the switching equipment, the storage, the method of operation in the arithmetic unit, the necessary index figures, the arithmetic speed and the control.

Mechanical office calculating machines work in the decimal system: Each counting wheel accordingly engages ten particular positions of the digits 0 to 9. With electronic computers it also seemed obvious at first to process

the figures directly in the decimal system in which the 10 digits are represented by 10 definite unequivocal electrical conditions, for example, through 10 current or voltage stages. Such a method, however, would be very unreliable because errors could easily occur through disturbances and changes in the control elements during their time of service or by fluctuations in the working voltages. To establish working reliability we make use initially of only two operating conditions, the most extreme ones possible, for example, the lit-up and extinguished low-voltage neon indicator lamp, current-carrying and blocked valves, positive or negative saturated magnetic cores, conducting or blocked semiconductor diodes, etc. With control elements working in this way, there are accordingly only two symbols available to represent and process the numbers, and the binary system with its two digits 0 and L²⁾ thus appears to be the obvious one, the more so as arithmetical operations can also be most easily effected in this system. Nevertheless, only one part of the electronic computer works in the binary system since this also has a number of drawbacks; above all, it is necessary for precise accuracy to have an index figure possibly three to four times greater in comparison with the decimal system, and conversion from or into the decimal system must be carried out each time at the input and output. The binary coded decimal system is therefore frequently used; in this the single digit x_i of the decimal system is coordinated with a binary digit $b(x_i)$ according to a specific instruction. We need at least four binary figures to be able to represent the 10 digits of the decimal system in this way through binary numbers. The appropriate four-figure binary numbers of the digits 0 to 9 are called coordinated *tetrads*. A range of machines also retains the

TABLE 2.1: BINARY CODED DECIMAL SYSTEM

Decimal digit	Direct (8-4-2-1)	Three excess	Coding Aiken (2-4-2-1)	Biquinary (4-3-2-1-0 5-0)	2 out of 5 (7-4-2-1-0)
0	0 0 0 0	0 0 L L	0 0 0 0	0 0 0 0 L 0 L	L L 0 0 0
1	0 0 0 L	0 L 0 0	0 0 0 L	0 0 0 L 0 0 L	0 0 0 L L
2	0 0 L 0	0 L 0 L	0 0 L 0	0 0 L 0 0 0 L	0 0 L 0 L
3	0 0 L L	0 L L 0	0 0 L L	0 L 0 0 0 0 L	0 0 L L 0
4	0 L 0 0	0 L L L	0 L 0 0	L 0 0 0 0 0 L	0 L 0 0 L
5	0 L 0 L	L 0 0 0	L 0 L L	0 0 0 0 L L 0	0 L 0 L 0
6	0 L L 0	L 0 0 L	L L 0 0	0 0 0 L 0 L 0	0 L L 0 0
7	0 L L L	L 0 L 0	L L 0 L	0 0 L 0 0 L 0	L 0 0 0 L
8	L 0 0 0	L 0 L L	L L L 0	0 L 0 0 0 L 0	L 0 0 L 0
9	L 0 0 L	L L 0 0	L L L L	L 0 0 0 0 L 0	L 0 L 0 0

²⁾ See 1), p. 4.

decimal system in which again purely binary information is used in the form of repeated pulses of equal amplitude.

2.2.1 THE BINARY SYSTEM

The advantage of the binary system lies in the fact that two digits are sufficient. According to the Equation (2.1) each figure is set down from the sum of the pure powers of the base 2, where all $x_n = 0$ or 1, in contrast to all other numeral systems. In complete accordance with the usual method of writing in the decimal system where each figure from right to left corresponds to a rising power of the base 10, each figure with a binary number represents a power of 2.

The binary number LL0L0.0L, for example, represents:

$$1 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 0 \times 2^0 + 0 \times 2^{-1} + 1 \times 2^{-2} = 26.25$$

A digit within a group of binary figures is called a Bit. Since in general every item of information is expressed through the combination of a specific number of binary instructions, the Bit serves as the unit of quantity of the information.

The addition of binary numbers takes place exactly as with decimal numbers so that after L+L, L must already be passed on to the next place. The following addition plan appears in consequence:

$$\begin{array}{r|ll}
 + & 0 & L \\
 0 & 0 & L \\
 L & L & L0
 \end{array} \quad (2.2)$$

Example 25 + 13:

	2^5	2^4	2^3	2^2	2^1	2^0
25		L	L	0	0	L
+ 13	+	0	L	L	0	L
38		L	0	0	L	L 0

2.2.2 BINARY CODED DECIMAL SYSTEM

Here the individual digits are binary coded according to an agreed code whereby the original index figure is maintained. In this way we exploit the advantages of the binary control elements for the decimal system without

being obliged to put up with the large index of the binary system and the intricate conversion from the decimal system to the binary system. Out of the great number of possible coordinations of tetrads $b(x_i)$ with decimal figures, only a few have any practical significance. Those most used are shown in the first three columns of Table 2.1. Special corrections are necessary here in order to calculate with these codings (see Section 2.2.3).

The **direct coding** with the weights 8, 4, 2 and 1 is the nearest instruction, namely

$$b(x) = x \quad (2.3)$$

Here each digit of the decimal system will also be directly translated into the binary system. In order to avoid difficulties in the tens-transfer mechanism with binary coded presentation in tetrads where the transfer to the next figure occurs at 15,

$$b(x_i) + b(x_k) = 15 \quad (2.4)$$

must be valid for the sum of two tetrads when the two decimal figures $x_i + x_k$ total 9. Direct coding does not possess this property, so other codings are frequently used.

We obtain the **three excess coding** (Stibitz) in which

$$b(x) = x + 3$$

It is distinguished among others by the fact that at no time can all four binary figures be 0 or L, a peculiarity which immediately shows the mistakes of the computer. A further advantage of this coding is the simple complement formation. The nine-complement of a negative number (see Section 2.3.1.1) is immediately produced here through interchange of 0 and L.

In order to facilitate computation of the represented digits from the tetrad, it must be possible to give a specific "weight" to each binary figure of the tetrad so that the weighted sum of the digits at once provides the decimal figure. This is the case with direct coding, but is not possible with the three excess code.

The **Aiken code** with the weights 2,4,2 and 1 fulfils this requirement and also the Relation (2.4). I corresponds from 0 to 4 to the direct coding, whilst 6 is added each time from 5 to 9:

$$b(x) = \begin{cases} x & \text{for 0 to 4} \\ x + 6 & \text{for 5 to 9} \end{cases} \quad (2.5)$$

It thus occurs that the fourth place of the tetrad is occupied from digit 5 and that after 9 (LLLL) the fifth place is added: here the occurrence of the

fifth place in the tetrad corresponds to the ten-transfer. The Aiken coding likewise facilitates the simple formation of the nine-complement through interchange of the 0 and L.

With **biquinary codings** we avoid the undesirable characteristic of binary coding in tetrads, namely that only 10 of the 16 possibilities can be utilised. A biquinary coded decimal number is composed of two parts: a five-place quinary part with the weights 4, 3, 2, 1 and 0, and a two-place binary part with the weights 5 and 0. The advantage of this coding lies in the simplicity with which it is possible to locate a fault. In the binary as well as in the quinary part, only one place can be in use at one time for one L. In comparison with other codings, the arithmetic unit is more complicated. The biquinary coding is important also in the indication of the decimal counter in computations in the pure decimal system. Here it has the advantage of easy readings without unreasonable trouble.

With the **2 out of 5 code** each decimal figure is represented by the combination of two pulses from a series of five whereby simple computing control is possible. The arithmetic unit is more complicated in this case.

2.2.3 COMPUTATION WITH TETRADS

With digital binary addition of decimal numbers coded in tetrads, the following difficulties occur: 16 different figures can be represented with a tetrad while we only need 10. That is to say, six combinations do not appear at all (e.g. with the Aiken coding the combinations 0L0L, 0LL0, 0LLL, L000, L00L and L0L0). These "pseudo tetrads" however, can occur in addition and the result then has to be converted into proper tetrads by a correction. The method of correction depends on the coding and on whether a decimal transfer has taken place or not.

With *direct coding*, addition always produces proper tetrads provided no ten-transfer has taken place, i.e. as long as the represented sum is less than 10. After a completed decimal carry-over, the figure 0LL0 (the binary 6) must be added as a correction appropriate to the six omitted combinations from 10 to 15. The following correction rule is then applicable:

Without ten-transfer: Correction 0
 With ten-transfer: Correction + 0LL0

In the *three excess coding* the figure 3 is carried forward in accordance with this rule by each addend; in the total, however, a further 3 should occur

when there is no ten-transfer, and a 9 (3 + 6) when a ten-transfer has taken place. The correction rule here is thus:

Without ten-transfer: Correction +LL0L
 With ten-transfer: Correction +00LL

A correction must always be introduced with the *Aiken coding* if a pseudo tetrad arises in addition. We must therefore always distinguish between two cases, depending on whether a decimal conversion has occurred or not. If a pseudo tetrad appears as the sum without decimal transfer, then the figure 0LL0 must be added since in this addition six combinations have been omitted. If a ten-transfer takes place, then in the coded system the number 16 would be carried forward in place of the number 10. Here the figure 0LL0 must thus be deducted from the total so that we obtain the following rule for the correction:

The sum is a true tetrad:	}	No correction
The sum is a pseudo tetrad:	}	Without ten-transfer: +0LL0
		With ten-transfer: -0LL0

Example: Addition in the Aiken coding: 36 + 55 = 91:

Decimal-system	ten	Coding	one
36 + 55	00LL L0LL		LL00 L0LL
	LLL0	Transfer L	L/0LLL ... Pseudo-tetrads
Correction:	—		—0LL0
91	LLLL		000L

2.2.4 CONVERTING THE DECIMAL TO THE BINARY SY

In machines which work in the pure binary system, the conversion into

binary numbers of the decimal numbers fed into the input proceeds in the following way. Each decimal digit is converted in direct coding into the appropriate tetrad (as in Table 2.1). In machines with fixed decimal point, each figure is a true decimal fraction which, with N places, in conformity with the Equation (2.1) has the form:

$$x = \sum_1^N x_k \times 10^{-k}$$

In this way each digit x_k is expressed as a directly coded tetrad so that the figure x has in all $4N$ binary digits. The machine now takes up these binary digits as a pure binary number, thus interpreting by it the number

$$y = \sum_1^N x_k \times 16^{-k}$$

which can easily be verified by a check. It thus has the task of computing the correct binary figure x from the "false" binary figure y . Since an undoubted connection exists between the two figures, the conversion can follow a fixed scheme depending on the binary index of the machine. Conversely, the translation of the binary results back into tetrads of the direct coded decimal system must take place at the output of the machine [7]. This relatively intricate conversion in addition to the big index is the reason why many machines do not use the pure binary system.

2.2.5 THE DECIMAL SYSTEM

If we wish to compute in the uncoded decimal system using binary information alone, we can then refer back to the counting of pulses in which each figure is represented by a corresponding number of pulses. If we were to allow these pulses to operate in chronological order, one after the other, we should then be faced with decimal numbers of several places with a considerable lapse of time for each calculation, since the chronological resolving of the circuit arrangements used in the computation is limited. We therefore employ parallel operation in which the individual decimal figures are allowed to run side by side, and each figure is counted separately so that we have a maximum of nine pulses per figure. The transfer to the next figure through suitable circuiting must then be considered. Fig. 2.2 shows an example of this presentation of figures. All four fundamental rules of arithmetic are here also reduced to addition which is brought about automatically through counting the pulses of the two addends. The "1 out of 10 code" can be used in the storage of decimal numbers. For each decimal figure of a number there is a storage unit with ten distinct places in readiness

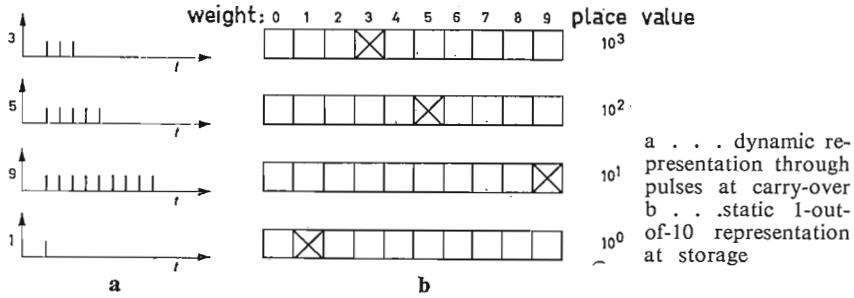


Fig. 2.2 Representation of the number 3 591 in the decimal system

to which we assign in turn the weights 0, 1, 2 . . . 9, as shown in Fig. 2.2b. We also frequently use the biquinary representation with the weights 4, 3, 2, 1 and 0 in the quinary part and 5 and 0 in the binary part, or else a coding in tetrads.

2.2.6 COMPARISON OF DIFFERENT NUMERAL SYSTEMS [9]

The different numeral systems have advantages and disadvantages depending on whether we have in mind the conversion at input or output, the method of operation in the arithmetic unit, the storage, the arithmetic speed, the complement formation, the necessary index figure or the possibilities for computing control. Table 2.2 gives a synopsis of the most important properties of the numeral systems mentioned.

TABLE 2.2: PROPERTIES OF DIFFERENT NUMERAL SYSTEMS

Numeral System	Index figure per decade	Suitable for	Unsuitable for
Binary	3.3	Computing Storage	Conversion at input and output
Binary coded (in tetrads)	4	Computing Storage	Computing control
Biquinary	7	Computing Computing control	Storage
Decimal	10		
2 out of 5	5	Computing control	Computing

So that we can work with convenient numeral systems, both in store and

in the arithmetical unit, for example, one numeral system is transformed in some machines into another inside the machine.

2.3 The fundamentals of computing in the arithmetical unit [5,7]

The working method of the arithmetical unit is distinguished in two senses compared with the usual calculations using the four basic rules of arithmetic: Firstly, all basic operations must be reduced to addition whereby two extra operations are necessary, the complement formation and the shift of place values, and secondly we are subjected to certain limitations or peculiarities with regard to the decimal point placing.

In digital computers the figures can only be represented through a finite index so that an additional place is necessary for the symbol. Depending on the handling of the decimal point, we distinguish three kinds of figure presentation: Machines with sliding, adjustable and fixed decimal point. In the last the decimal point is fixed within the available index figure in the column of digits and all problems to be solved by the machine must be adapted through suitable regulation of this decimal point placing in order to avoid an overflow of the store and arithmetical unit. With the sliding decimal point, on the other hand, the position of the decimal point adjusts itself to the order of magnitude of the figures fed in and obtained during the computation. With machines with adjustable decimal point, the place of the decimal point can be moved within certain limits inside the column of figures.

2.3.1 COMPUTING WITH FIXED DECIMAL POINT

Here a definite place is indicated for the decimal point for all numbers. With many machines the decimal point stands at the beginning; they also work with proper fractions. This means that all computation quantities in the range $-1 < x < 1$ must be transformed. This causes no difficulties if the order of magnitude of the figures appearing and expected is known to some extent, as for example in commercial problems. Since the decimal point is fixed, it needs no special symbol; we have to imagine it for each figure to the left before the first place. If, for instance, the figure π is to be used in the machine, it must first be transformed into the range of the machine to 0.314159 through division by 10; in a five-figure machine it is represented by 31416.

2.3.1.1 *Addition and subtraction*

The true significance of an addition or subtraction to be carried out can only be appreciated after considering the symbol of the operants. We therefore treat addition and subtraction on an equal basis whereby only

the symbols are appropriately taken into account. Here the negative figures in the arithmetic unit will not be represented as an absolute total with the negative symbol, but as the complement, while a constant C will be automatically added to each negative number x which goes into the arithmetic unit. The sum of the two

$$x = x + C \tag{2.6}$$

is called the complement of x. The subtraction of x is then carried out by the addition of the complement \bar{x} .

If we choose for C the base B (B-complement) then, if the positive figures are proper fractions, the negative figures will become improper fractions so that the register must have yet another place before the decimal point. Since the carry-over of the ones is disregarded, the 0 appears as a positive figure.

Example: Subtraction of the two numbers +0.568 and +0.437:

Storage unit	Arithmetic unit
+568	0.568
-437	+9.563 ... complement formation
+10	0.131 ... total

As this example in the decimal system shows, the process of subtracting figures of several places means the formation of the ten-complement (B-complement) for the lowest place and of the nine-complement ((B-1)-complement) for the remaining places. With the (B-1)-complement, the difference between the base and the unit η of the last place of the number is selected as the constant C:

$$C = B - \eta \tag{2.7}$$

Zero is here counted as a negative figure since now $C < B$, so that no reduction to zero results as a consequence of the absence of the carry-over. The zero remains in the register rather as an improper fraction (B- η), that is to say, as a negative figure. It thus comes about that the complement formation in the total can again be disregarded. When carrying out subtraction it can thus happen that the (B-1)-complement is formed from all places of the subtrahend and the carry-over of the ones to the lowest place as a result of the addition is taken into account.

Example: Subtraction of the number 0.437 from 0.568:

$$\text{Here } C = B - \eta = 10 - 0.001 = 9.999$$

Storage unit	Arithmetic unit
+568	0.568
- 437	+9.562 ... complement formation
	+9.999
	10.130
	L → +1
	0.131 ... difference

Since the various binary coded numeral systems allow simple formation of the nine-complement through interchange of L and 0 (see Section 2.2.2), we work conveniently here with the $(B - 1)$ -complement according to the above example.

2.3.1.2 Multiplication

In a computer which works in the numeral system with the base B , the multiplicand x and the multiplier y will, according to Scheme (2.1) be brought out of the storage unit in the following form:

$$x = \pm \sum_1^N x_k \times B^{-k} \quad \text{or} \quad y = \pm \sum_1^N y_k \times B^{-k}$$

whereby the x and y can take the values $0, 1, 2, \dots, B - 1$ and N is the index figure of the machine. The maximum N -place result can be built up electronically in two ways: First we can form and total up all the partial results $x_k y_l$:

$$xy = \sum_1^N x_k y_l B^{-(k+l)} \quad (2.8)$$

The result is here composed of N^2 partial results. A second possibility is to multiply the whole multiplier y successively by the single x_k of the multiplicand and then total up these partial results:

$$xy = \sum_1^N x_k y B^{-(k+1)} \quad (2.9)$$

With series machines and in multiplication with the multiplication table units, the work is carried out according to Scheme (2.8), with parallel machines according to (2.9). There are various possibilities for obtaining the partial result:

- a) Continuous totalling of y (as, for example, in office calculators).
 b) First of all, all multiples of y ($2y, 3y \dots, (N-1) \times y$) are formed by totalling up, and these results are stored in the registers. Then the real multiplication begins according to (2.9) by bringing up $x_k y$ from the appropriate registers.
 c) Only every second multiple of y ($2y, 4y \dots$) is produced and the remaining multiples can then be obtained by an extra addition of y .

The formation of the partial results is very simple in the binary system: in each arithmetical step x will not be fed into the accumulator at all ($x_k = 0$) or only once ($x_k = 1$). This easy computation of the result is an added advantage of the binary system.

The number of additions necessary for a multiplication in an N -place machine depends on the way the results $x_k y$ are produced.

Formation of the partial result according to	a)	b)	c)
Series working method (2.8)	average $4.5 N^2$ maximum $9 N^2$	$N(N + 8)$	$N(2N + 2)$
Parallel working method (2.9)	average $4.5 N$ maximum $9 N$	$N + 8$	$2N + 2$

In the binary system in case a) the average only needs $N/2$ additions; however, since the index here is about 3.3 times greater than the decimal index N , the number of additions needed for a multiplication is $5.5N^2$ or $1.7 N$.

The accumulator must have $2N$ places to ensure that there is no error in the last essential place through omitting the inessential places of the result. We can manage $N + 1$ places in the accumulator, however, if we proceed as follows: Beginning with the highest place, we form successively the expressions

$$\begin{aligned}
 p_N &= 0 \\
 &\vdots \\
 p_{k-1} &= B^{-1} (p_k + x_k y) \quad (k = N, N-1, \dots, 1) \\
 p_{k-2} &= B^{-1} (p_{k-1} + x_{k-1} y) \\
 &\vdots \\
 p_0 &= xy
 \end{aligned} \tag{2.10}$$

The last step p_0 produces the result. Thus the $(N+1)$ places ($B^0, B^{-1}, \dots, B^{-N}$) of p_k in the adding device (the accumulator) and the N places ($B^{-(N+1)}, \dots, B^{-2N}$) of the result $x_k y$ are stored in the register of the arithmetical unit.

The formation of the results $x_k y$ is very simple in the binary system. The scheme (2.10) here takes the form:

$$p_{k-1} = \begin{cases} \frac{p_k}{2} & \text{if } x_k = 0 \\ \frac{p_k + y}{2} & \text{if } x_k = L \end{cases} \quad (k = N, N-1, \dots, 1) \quad (2.11)$$

The calculation of p_{k-1} now proceeds in the accumulator by adding the suitable multiple $x_k y$ from the index to the p_k remaining in the accumulator and the multiplication by B^{-1} is then carried out by moving one place to the right. After reaching p_0 the multiplication is complete. The result with its first N , the essential places, is in the accumulator.

Example: Three-figure decimal system.:

Step	Register (N places)	Accumulator ($N + 1$ places)
p_3	000	0000
$p_3 + 7y = 10p_2$	369 ... 7y	3690
p_2	369	0369
$p_2 + 0y = 10p_1$	000 ... 0y	0369
p_1	000	0036
$p_1 + 3y = 10p_0$	158 ... 3y	1616
$p_0 = xy$	158	0161

2.3.1.3 Division

In the division $z/y = x$, it is necessary to make sure that $z < y$ so that the amount of the quotient remains less than 1. (In some cases a shifting of place values is required). A method frequently used in division is the conversion of the multiplication process according to Equation (2.10). In this way we obtain

$$\begin{aligned} p_0 &= z \\ p_k &= B p_{k-1} - x_k y \quad (k = 1, 2, \dots, N) \\ p_N &= B^N \text{ times the remainder.} \end{aligned} \quad (2.12)$$

To carry out this computation p_0 is brought into the accumulator and moved one place to the left (by B) and y is deducted until a negative figure appears in the accumulator. Then the positive remainder is restored again by adding y . Now p_1 in the accumulator is moved one place to the left and y again deducted, and so on continuously. The x_k amount of the deducted y is

stored in the register after each step and moved one place to the left so that here after reaching p_{n-1} the quotient appears while B^N times the remainder is in the accumulator. This process is simplified in the binary system because here y can only be deducted once at the most.

Example: Three-place decimal system:

Step	Accumulator	Register
p_0	0403	000
$10 p_0$	4030	000
$p_1 = 10 p_0 - 5 y$	0425	005
$10 p_1$	4250	050
$10 p_2$	6450	550
$p_3 = 10 p_2 - 8 y$	0682	558

Not all computers are equipped for carrying out division directly. In such cases the division is reduced to multiplication with the reciprocal value of the divisor y , obtained according to Newton's method (corresponding to Section 2.1.1): We assume an initial solution z_0 of $z = 1/y$ and then obtain the first approximation from

$$z_1 = z_0 (2 - y z_0)$$

The machine can thus work cyclically according to the relation

$$z_{n+1} = z_n (2 - y z_n)$$

as long as the necessary accuracy for $1/y$ is achieved.

2.3.2 MACHINES WITH SLIDING DECIMAL POINT

The introduction of the sliding decimal point is necessary when the figures to be worked and the intermediate result are differentiated about the power of 10 as can be the case in many scientific and technical problems.

In these computers all digits are represented in the so-called semi-logarithmic form

$$x = \pm p \times B^q \quad (2.13)$$

Here B is the base of the numeral system in use, p the mantissa which lies constantly in the interval $1 \leq p < B$ and q the exponent which indicates the place value.

It must be noted in addition and subtraction that only numbers with equal exponents can be added; as a rule therefore, there must first be a place value shift to the right with smaller addends, that is by the difference of the exponents of the two addends. If the mantissa of the total is greater than the base, another adjustment of the total must be made through a shift of place value.

In multiplication and division the exponents are added or subtracted respectively and the mantissas multiplied or divided. In this way the mantissas of the product can lie between 1 and B^2 and of the quotients between B and B^{-1} , so that here also a shift to the right is necessary with the product and to the left with the quotient.

The fundamental rules of arithmetic required in this method of computing are carried out in the same way as in machines with fixed decimal point.

2.3.3 COMPUTING CONTROLS [91, 92, 93, 94]

It is in the nature of things that components in a computer can occasionally break down so that the machine makes mistakes. The computer must be so constructed that these mistakes occur as seldom as possible, and that if occasion arises, they will be quickly traced. A series of computing controls has therefore been developed which continuously supervises the computing process.

- a) With sufficiently smooth functions suitable subtractions bring the mistake into view.
- b) Through appropriate instructions each computing step is carried out twice in different ways, which increases the computing cost about three-fold.
- c) The output values from each calculation are re-calculated and compared. This also means about three times the computing cost.
- d) One problem is calculated simultaneously on two equal machines running parallel and the intermediate results are automatically and constantly compared from step to step.
- e) In machines with binary coding or with the 2 out of 5 code, the figures can be checked by seeing that each number contains two binary L and no more.
- f) Special control digits with a definite relation to the digits of the number are added to the binary digits of the numbers so that the original number can be deduced from the control number according to definite rules used in detecting an error.

2.4 The fundamental circuits [10, 11]

2.4.1 THE LOGICAL CIRCUITS

In binary addition according to plan (2.2), the following connecting rules exist between the two binary digits:

$$\begin{array}{rcl}
 & \text{Total} & \text{Carry-over} \\
 0 + 0 & = 0 & \dots\dots\dots 0 \\
 L + 0 & = L & \dots\dots\dots 0 \\
 0 + L & = L & \dots\dots\dots 0 \\
 L + L & = 0 & \dots\dots\dots L
 \end{array} \tag{2.14}$$

These connections can be realised through suitable combinations of three simple basic circuits. Because of the binary character of the number processing in computers, we can refer to formal logic for their mathematical treatment (see, for example [77, 79]) by regarding value 0 as correct information and value L as incorrect information. Because the three necessary basic circuits in this sense produce logical information they are called logical circuits. Here we can distinguish circuits with one or several inputs. Logical circuits with several inputs and one output are termed *gates*.

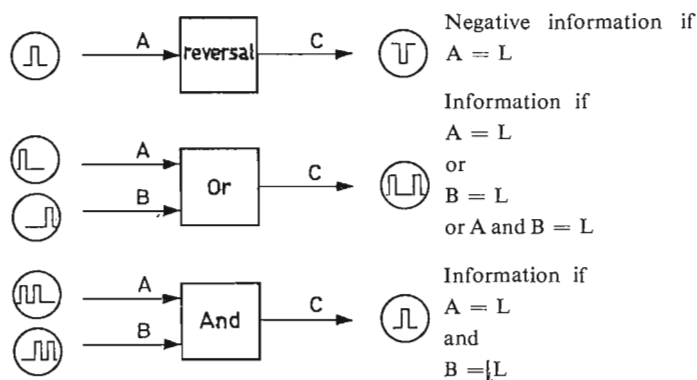


Fig. 2.3 The logical fundamental circuits

In detail we are concerned with the following three circuits:

- The reversal circuit:* A positive pulse at the input gives a negative pulse at the output.
- The Or-gate (disjunction):* A circuit with several inputs and one output

which supplies one output pulse when a pulse occurs at one or several inputs.

- c) *The And-gate* (conjunction): A circuit with several inputs and one output which only supplies an output pulse when all the inputs are simultaneously reacting.

These three circuits are shown in diagram form in Fig. 2.3 (the And- and Or-gates as special cases with two inputs).

We can use the And-gate for the carry-over to the next binary figure where we need information for $L+L$. For the remaining connections (2.14), however, we require a circuit which gives a pulse if there is a pulse at either one or the other of the inputs, and supplies no information if a pulse occurs at both inputs. A circuit of this type (*Either-or-gate*) is easily obtained by combination of the three fundamental circuits as is shown in Fig. 2.4.

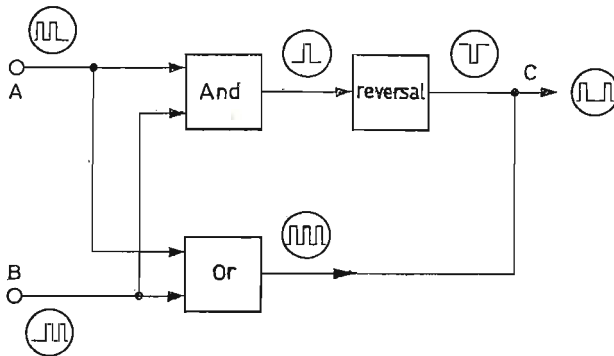


Fig. 2.4 Exclusive Or-gate

When a pulse is only present at A the And-gate is blocked and the Or-gate supplies information at C. If there are pulses at A and B, the And-gate and the Or-gate supply information; the pulse of the And-gate, however, is also reversed in polarity so that no information occurs at C. Finally the Or-gate yields an output pulse when B alone receives a pulse.

The *Inhibit-gate* is a further combined logical circuit. As a rule it has $n+1$ inputs and delivers information when pulses occur at n inputs. We are thus dealing here with an And-gate whose coincidence can be cancelled through an additional input. The circuit can be built up from an And-gate with $n+1$ inputs and a reversal stage at one input (see Fig. 2.5). Input $n+1$ of the And-gate is at a grid potential corresponding to the transmission voltage so that pulses at the remaining inputs A_1 to A_n produce information. If input A_{n+1} is also addressed the grid potential at the And-gate is cancelled

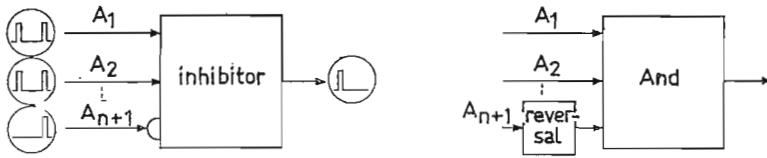


Fig. 2.5 Inhibit-gate

by the reversal stage, and the coincidence of the n inputs is cancelled. In practical operation it must be ensured that the time of the pulse at input A_{n+1} covers that of the remaining input pulses.

If all the inputs of an And-gate are biased with the transmission potential and provided with reversal stages, we obtain the Nor-gate. This corresponds to a reversed Or-gate. It gives information when no input is addressed and supplies none when pulses operate at one or more inputs. As well as the binary connections, the basic circuits have numerous other uses in computers. In addition to the comparison of two figures, the information of which is to influence the further progress of the computation in the required direction, the And-gate is primarily used as a switch to set up the connections for figures and instructions; it makes the electronic substitute for a relay as is shown in Fig. 2.6.

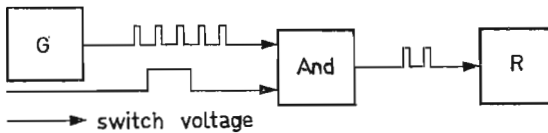


Fig. 2.6 And-gate as externally controlled switch

In this example a definite number of pulses is to be sent from the master clock G into the arithmetical unit R . The clock feeds the one input of the gate. No pulse can pass as long as potential necessary for the coincidence is missing at the other input. The And-gate is only "switched on" through the transmission voltage at the second input and allows pulses to pass during its operating period.

When pulses from different lines have to be brought into a common line, the Or-circuit is frequently used as a pulse mixer to avoid mutual reaction between the individual circuits.

2.4.2 BISTABLE AND MONOSTABLE CIRCUITS

Bistable and monostable flip-flop circuits are of great importance in elec-

tronic computers. Fig. 2.7 shows a mechanical analogue for this type of circuit. The bistable flip-flop circuit corresponds to a two-pole circuit which can be switched over between the two stable positions I and II and thus between the potentials V_1 and V_2 by brief triggering at a or b. With the monostable flip-flop circuit only position I, shown as an unbroken line, is stable.

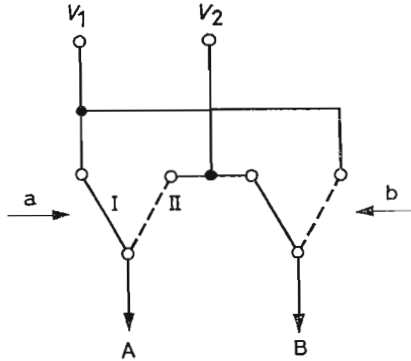


Fig. 2.7 Analogue of a flip-flop circuit

Through a short pulse at input a the switch triggers over to the quasi-stationary position II, remaining there for a definite time to revert from there to the stable position again. The bistable multivibrator (Flip-Flop, Trigger, Eccles-Jordan Circuit) and the monostable multivibrator are chiefly used for these trigger circuits in computers.

In the *bistable multivibrator* we have a circuit with two inputs and two outputs, so that only two stationary conditions are possible: Either output A has a high voltage and output B a low voltage (“even condition”), or the reverse is the case (“odd condition”), as Fig. 2.8 shows. Inputs a and b are so coupled to the outputs A and B that a negative pulse at b produces the odd condition from the even one, and a negative pulse at a turns the odd into the even condition. These conditions also persist after

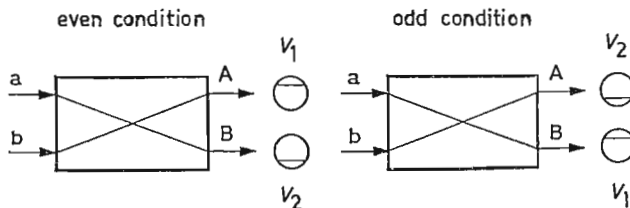


Fig. 2.8 Representation of the two conditions of the bistable multivibrator

the cessation of the switch-over pulse. The bistable multivibrator is consequently suitable for transforming short pulses into static voltages, which is the reason for its use in counting and storage circuits. If the bistable multivibrator is again triggered over after a time T , its outputs supply one positive and one negative pulse of duration T so that it can also be used for the production of square-wave voltages whose duration or gap is marked by the interval between two short pulses. Since two input pulses are required to generate a square-wave pulse at one output the bistable multivibrator simultaneously provides a pulse reduction of 1 : 2. As it changes a short pulse into static information, it also carries out a storage function.

The *monostable multivibrator* is a circuit similar to the bistable multivibrator but it has only one stable condition. Through a suitable release pulse this circuit triggers over from this stable condition into an intermediate one, to revert after a certain time to the stable starting condition (Fig. 2.9).

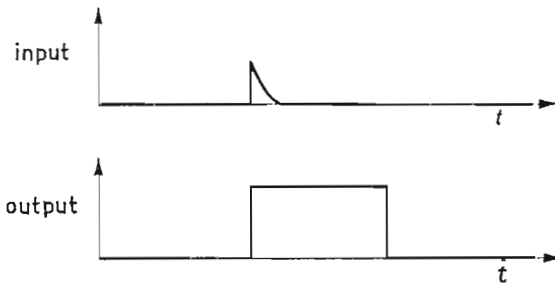


Fig. 2.9 Principle of the monostable flip-flop circuit

Such circuits are chiefly required for forming, regenerating and retarding pulses. A pulse former serves to produce a specific pulse form from any pulse within certain limits. We have this task, for example, in pulse counting where a pulse form convenient for the counting circuit must be produced from input pulses occurring in more or less random form, or when a square-wave voltage of definite duration has to be obtained from time markings given by needle pulses.

By *pulse regeneration* we understand the process of renewing the form of a pulse which has been distorted during the computation (e.g. in delay cables). Here the distorted pulse can serve as a release for the monostable multivibrator which in turn yields a pulse of the original form at the output.

In *pulse retardation*, the pulse to be delayed releases the monostable flip-flop circuit. After the desired retarding time the circuit then triggers

back to the resting condition; the pulse flank so obtained then gives up the delayed pulse through, for instance, a differentiation (Fig. 2.10). The pulse produced by the first flank can be suppressed by a diode.

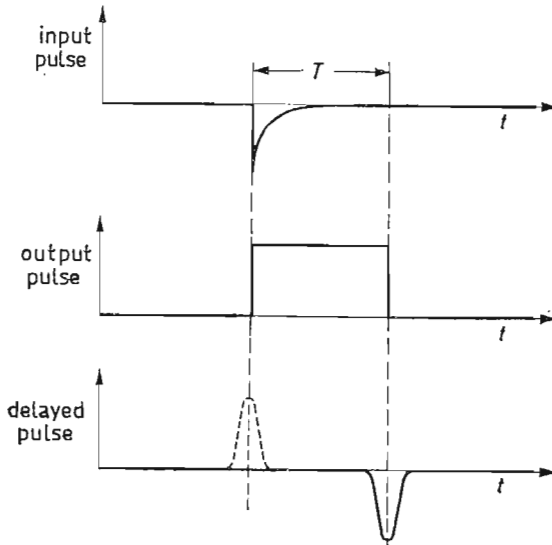


Fig. 2.10 Principle of a delaying circuit

2.4.3 COUNTING CIRCUITS

A counter for numbers in the system with the base B is a circuit which can take in B different stable conditions which run through one after another when B pulses are fed into the input. A carry-over pulse is given at the output with each B th pulse. Great numbers of decimal (or decade) counters ($B = 10$), for instance, are needed in computers which work in the uncoded decimal system. If we disregard the special counting tubes, an electronic counter is made up of a chain of bistable components connected one after the other; the bistable circuits thus offer a guarantee of the required working reliability. Each condition of the counter is composed of a definite combination of binary informations according to the position of the individual bistable components; the digits fed in as a pulse series are indicated in code. The characteristic property of the counter, apart from its working reliability, is its maximum counting speed which determines the speed of the arithmetical unit. It depends chiefly on the components used and is about 20 Mc/s for triodes, between 100 kc/s and several Mc/s for transistors and ferrite stores and about 2 kc/s for trigger tubes. At the same time, the demand for

energy and space as well as the outlay for other switching equipment (e.g. for visible indication of the circuit condition) are important considerations.

There are two fundamentally different methods of pulse counting: In one the pulses are binary counted; then each stage of the counting apparatus is coordinated to a binary figure and the places of the single stages ("0" or "L") then give the number of the counted pulses. We can, however, use the so-called ring counter. With this there is only one binary element at a time in position "L". Through each input pulse, this unique "L" condition is passed on from stage to stage until after B input pulses it appears again in the first stage. With binary counting, only numeral systems with the base 2^n can be directly realised. (n . . . number of binary elements). Therefore additional circuit arrangements are necessary for the decimal system. This difficulty does not occur with the ring counter since it has n different positions with n components.

As well as the decimal counting circuits composed of bistable components, there is a range of decimal counting tubes with ten different direct conditions. Gas-filled tubes are suitable for counting pulses up to more than 100 kc/s series frequency. Here we have cold cathode tubes with one anode, 20 grids and 10 cathodes [49]. The vacuum counting tube E 1 T [29], a special electron beam tube with ten stable beam positions, allows the counting of pulse series up to 100 kc/s. The trochotron [50], a magnetic field tube, counts pulses up to more than 1 Mc/s series frequency.

2.4.3.1 Feedback decade counters (tetrad counters)

Fig. 2.11 shows the basis of pulse counting with a binary chain consisting of four bistable multivibrators M_0 to M_3 . Each stage operates as a 1 : 2 reducer. The binary chain thus produces the conditions shown in Table 2.3 where the weights 1, 2, 4 and 8 belong in sequence to the individual bistable elements. The decimal number 13, for example, corresponds to the binary number LL0L. Since M_3 only gives a negative pulse after 16 pulses, the binary chain operates at the same time as 1 : 16 reducer (as a rule, with n bistable components, 1 : 2^n).

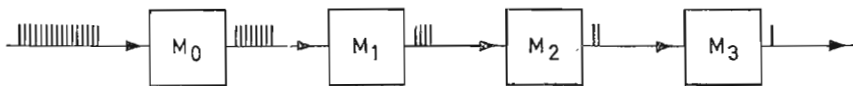


Fig. 2.11 Binary chain for pulse counting

TABLE 2.3: CONDITIONS OF A BINARY CHAIN OF FOUR BISTABLE COMPONENTS

	Pulse number																Weight	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		16
M_0	0	L	0	L	0	L	0	L	0	L	0	L	0	L	0	L	0	1
M_1	0	0	L	L	0	0	L	L	0	0	L	L	0	0	L	L	0	2
M_2	0	0	0	0	L	L	L	L	0	0	0	0	L	L	L	L	0	4
M_3	0	0	0	0	0	0	0	0	L	L	L	L	L	L	L	L	0	8

To obtain a decade counter from this type of four-stage reducer we have to ensure that the chain can take in only 10 conditions instead of 16, i.e. six places must be passed over. This is done by an appropriate return from the last stages to the first which can be undertaken in various ways. We can count up to 7 normally, for instance, and introduce the feedback through the eighth pulse. In accordance with Table 2.3 the eighth pulse produces the reversal of stage M_3 from 0 to L. If we use the pulse produced by this reversal to convey stages M_1 and M_2 to position "L" by a feedback, the counter is now in the condition "LLL0" (i.e. in the binary 14) so that after two further pulses the counter has already reached the zero condition.

$M_3M_2M_1M_0$

L 0 0 0 ... Condition after 8 pulses without feedback

L L L 0 ... Condition after 8 pulses with feedback to M_1 and M_2

L L L L ... Condition after 9 pulses

0 0 0 0 ... Condition after 10 pulses

With this feedback, the coding of the decimal figures is binary for the digits 0 to 7 while the 8 corresponds to the binary 14 and the 9 to the binary 15. With this method of feedback, it is thus impossible to give a fixed weight to single stages.

The feedback shown in Fig. 2.13, on the other hand, gives an indication of the counting situation in direct binary coding (see Section 2.2.2), the stages having the weights 8, 4, 2 and 1. This counter thus works up to the 9th pulse in complete agreement with Table 2.3.

At the 10th pulse the remaining six positions must then be jumped over and the counter brought to the zero position. This is carried out through the two extra coupling lines A and B. Line A goes from the output of stage

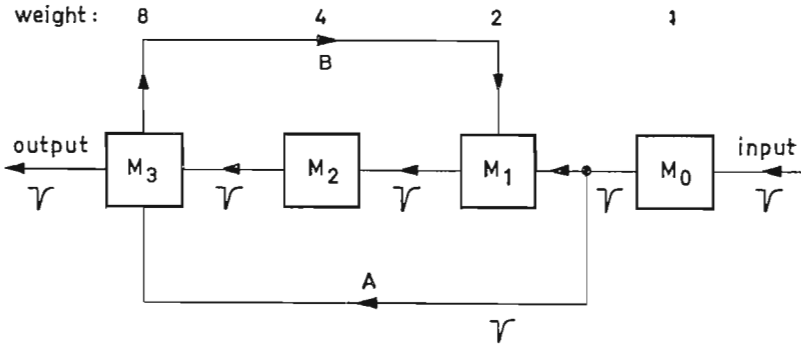


Fig. 2.12 Decade counter with direct binary coding

M_0 to stage M_3 ; here the coupling is done in such a way that a positive pulse has no effect and a negative one is only effective when M_3 is in position "L". The feedback B causes a blocking of the chain from stage M_1 if M_3 is in position "L". Then the circuit works up to the 9th pulse according to Table 2.1 (Condition: L00L) since the two coupling lines have no influence up to there. With the 10th pulse M_0 is reversed from L to 0; the negative pulse thus produced has no influence in M_1 because of the blocking by B. A return from M_3 to 0 is brought about, however, (by an output pulse) so that all stages are now in position 0. Another counter working in the Aiken code will be discussed in the description of special circuits.

The maximum counting frequency of a binary counter is limited by the release capacity of the first stage since the second stage receives only half the input frequency. With decade counters in general, however, this maximum counting frequency is reduced by about the factor 0.75 through the feedback required. If the feedback is to the second stage, for example, only the period corresponding to half the counting frequency is available for the feedback process.

2.4.3.2 Ring counter [51]

This consists of a circular arrangement of coupled bistable components, as shown in Fig. 2.13. The pulse series to be counted is fed simultaneously at all inputs of the bistable components. It is characteristic of this arrangement that of all the n bistable components, only one at a time is in position "L", while the rest are condition "0" so that through each input pulse the condition "L" passes on to the next component.

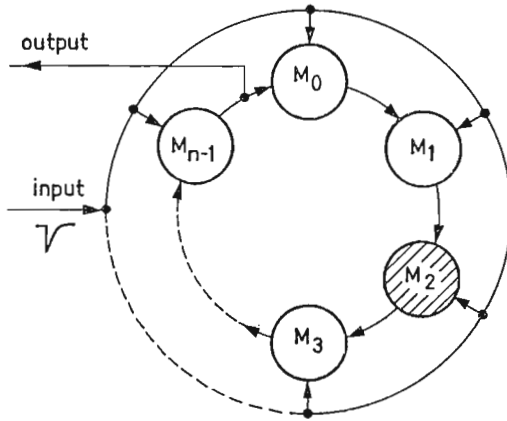


Fig. 2.13 Principle of the ring counter (in position 2)

For an arrangement like this the bistable components must have the following properties:

- The input pulse does not influence the component in position "0".
- The output pulse triggers the component in position "L" over to "0".
- The output pulse thus produced (transfer $L \rightarrow 0$) triggers the subsequent component over into condition "L".
- The output pulse corresponding to this reversal does not influence the succeeding component (transfer $0 \rightarrow L$).

Ten bistable components are used here for one decade (compared with four in binary counting). In this way we give each stage in sequence the weights 0, 1, 2, ..., 9 and then obtain the number of input pulses in the "One-out-of-ten-presentation" (see Section 2.2.5). The condition of this type of ring counter can easily be read, for instance by indication with neon lamps.

By replacing the "One-out-of-ten-figure-presentation" by a biquinary presentation (see Section 2.2.2), we still only need six bistable components for one decade, as Fig. 2.14 shows. The actual counting ring here consists of five components (M_0 to M_4) which have in turn the weights 0 to 4 while the weight 5 belongs to the additional bistable component.

The Five-ring corresponds to the arrangement in Fig. 2.13. The output pulse from M_4 additionally feeds the bistable component M_5 which is switch-

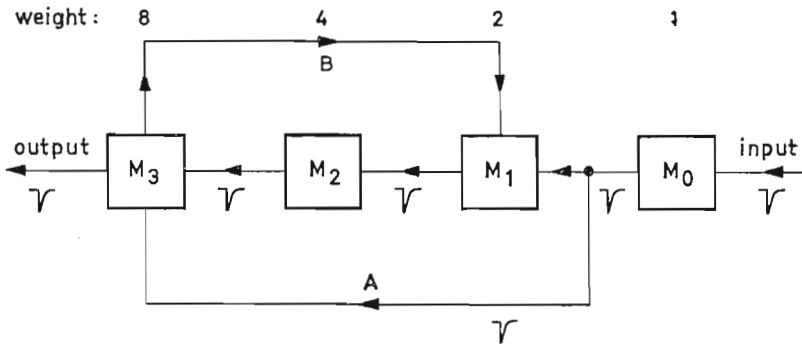


Fig. 2.12 Decade counter with direct binary coding

M_0 to stage M_3 ; here the coupling is done in such a way that a positive pulse has no effect and a negative one is only effective when M_3 is in position "L". The feedback B causes a blocking of the chain from stage M_1 if M_3 is in position "L". Then the circuit works up to the 9th pulse according to Table 2.1 (Condition: L00L) since the two coupling lines have no influence up to there. With the 10th pulse M_0 is reversed from L to 0; the negative pulse thus produced has no influence in M_1 because of the blocking by B. A return from M_3 to 0 is brought about, however, (by an output pulse) so that all stages are now in position 0. Another counter working in the Aiken code will be discussed in the description of special circuits.

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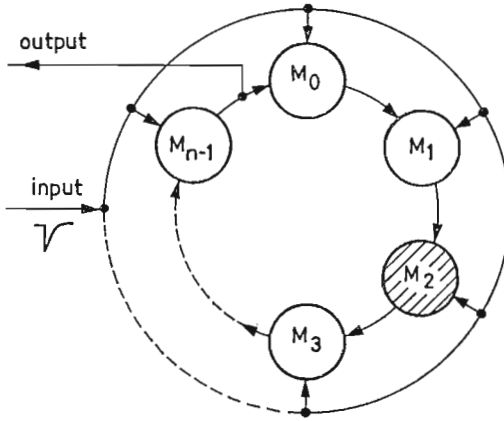


Fig. 2.13 Principle of the ring counter (in position 2)

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- The output pulse corresponding to this reversal does not influence the succeeding component (transfer $0 \rightarrow L$).

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By replacing the “One-out-of-ten-figure-presentation” by a biquinary presentation (see Section 2.2.2), we still only need six bistable components for one decade, as Fig. 2.14 shows. The actual counting ring here consists of five components (M_0 to M_4) which have in turn the weights 0 to 4 while the weight 5 belongs to the additional bistable component.

The Five-ring corresponds to the arrangement in Fig. 2.13. The output pulse from M_4 additionally feeds the bistable component M_5 which is switch-

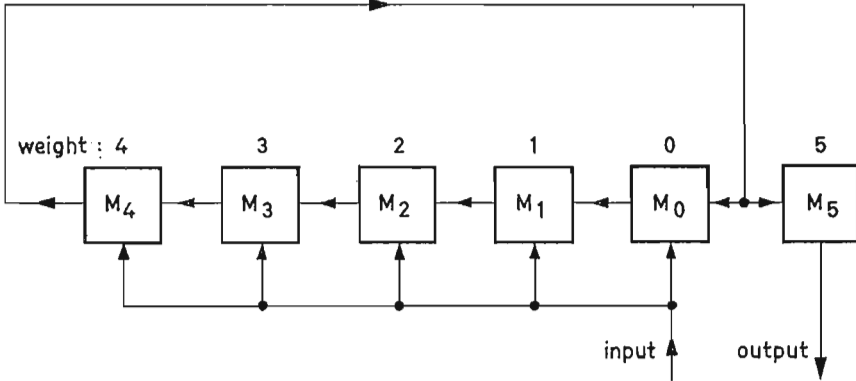


Fig. 2.14 Biquinary ring counter

ed over by each pulse coming from M_4 . In the zero position M_0 is in condition "L", and all the remaining components, including M_5 , are in condition "0". After the 5th pulse M_0 is again in condition "L". At the same time, however, M_5 has been brought into position "L". The 10th pulse then triggers M_5 back into zero position. The pulse thus produced operates as output pulse of the circuit.

2.5 The electrical presentation of figures

Figures are always represented in computers by binary information: all figures occurring in the machine are expressed through two different voltage values. Here there are two possibilities:

- The two binary symbols 0 and L correspond to different voltage values: we talk of static representation as supplied, for example, by the bistable multivibrator (number storage).
- The two symbols 0 and L are expressed periodically through the presence or absence of pulses at certain places. The pulses follow at interval τ with a pause between pulses (Transport and handling of numbers).

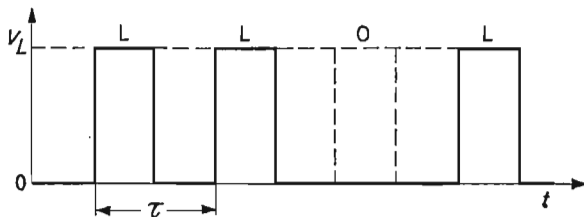


Fig. 2.15 Representation of the number LL0L through a pulse series

The signals which represent the digits of a number can be transmitted in various ways in the computer. They can pass along one line in periodic succession (series operation), or each figure of the number can go simultaneously along a separate line (parallel operation). In a series machine the next number follows when all the digits of one number have been passed through. Fig. 2.16 shows the pulse series for two ten-figure decimal numbers. The interval between two digits is the pulse period τ , that between two numbers the number period T . We see at once that in the binary system multiplication by 2^n or division by 2^n corresponds to a shifting of the places by n pulse periods to right or left respectively.

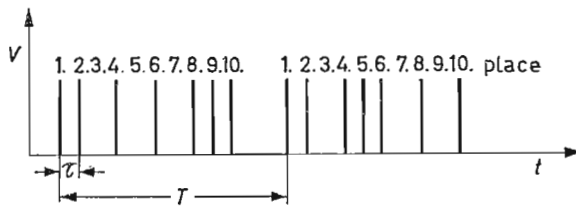


Fig. 2.16 Number presentation in a ten-digit binary series machine

With machines working in the binary coded system, the numbers can be treated in three ways (e.g. by tetrad coding): Tetrad pulses and digits in series (one line), tetrad pulses in parallel and digits in series (four lines) and finally tetrad pulses and digits in parallel (number of lines equal to four times the number of places).

In a series machine the pulse series corresponding to an inserted number can be produced in the following ways (see Fig. 2.17): The master clock gives pulses with the series period τ . We also require a number of And-gates, A_0 to A_{n-1} whose inputs are fed one at a time through the master clock. The other inputs are fed from the outputs of the preceding And-gates over a delay section DS, with a delay of one pulse period. This process is periodically repeated so that at the second input of A_0 , pulses obtained from the master clock through frequency division operate with the number period T . Then each output of the gates supplies a pulse shifted by τ which corresponds to one place of the binary number. These outputs are now passed again to a second chain of And-gates A_0' to A_{n-1}' , whose outputs are brought together. For each digit L occurring in the number to be represented, only the appropriate gate needs to be open via the second input (e.g. through punched card control).

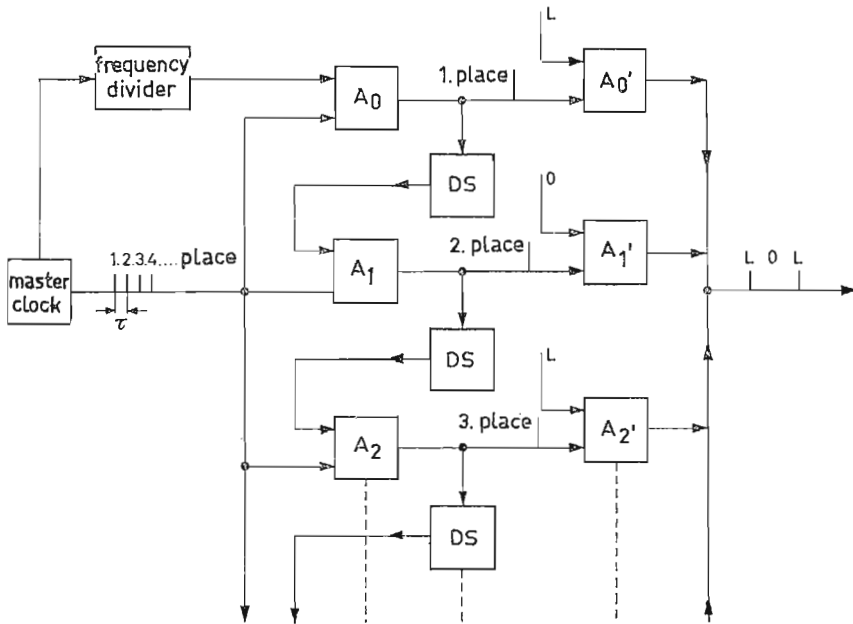


Fig. 2.17 The production of the binary number LOL in a series machine

2.6 Storage systems [9, 11, 20]

As we have already seen in the description of the working method of the automatic calculator (see Section 1.3), subsidiary storage units are necessary in addition to the main store in the electronic digital computer. The automatic operation of the electronic computer is based to a great extent on the property of the storage unit of holding numbers and computing instructions and giving them up again when required.

The demands made on the various storage units largely depend on the problem they have to solve inside the machine. For example, while the main store must be suitable for receiving a great mass of information, a register in the arithmetical unit only needs to take in one number at a time, though the figures must be quickly available again to achieve great arithmetical speed. We have thus indicated the two characteristic properties of a store: the capacity for information and the access time. The capacity of a store tells how many bits (yes-no-values) it can take. To keep n different conditions in one store, we need the capacity

$$C = {}^2\log n$$

The access time refers to the period necessary to make certain information available, i.e. the time which passes between the summoning of a certain storage cell and the flowing of its contents into the arithmetic unit. The access time must be adequate in proportion to the arithmetical speed. The storage capacity limits the extent of the computation which can be accomplished without readjustment of the machine, and the access time governs the arithmetical speed.

A storage unit is also marked by its production costs, taking into account the outlay for subsidiary circuits, and by its working reliability. Up to now there is no known storage principle which solves all problems satisfactorily, and for a definite objective we have to confine ourselves to finding the most convenient method of operation from the various storage possibilities. Since storage is always done binarily, the store must be composed of a certain number of components adapted to binary information ("binary cells").

The working methods of digital stores known at present are derived from three physical principles [12]:

1. In *structural stores* the electrically written information is converted in structure-changing solid bodies, as for example, in ferromagnetic and ferro-electric materials or in the photographic layer. Structural stores, however, only need energy for writing and not for holding information and therefore they offer great storage density in relation to space.
2. In *energy stores* the information produces certain energy conditions which persist for a given time, as for example, the electrostatic energy in capacitors or the energy in mechanical oscillating fields, e.g. in magnetostrictive materials. If the information has to remain stored over a long interval, it must be periodically re-written (dynamic store). Energy stores thus rely on continuous energy supply.
3. With *feedback stores* two or more stable conditions are produced through an outer or inner feedback. This is the working method of the bistable circuits, the cold cathode trigger tubes, the counting tubes, the point contact transistors and storage tubes with a holding device. These stores also need a continuous (static) energy supply.

Stores which rely on continuous energy supply have the disadvantage that they lose their contents if a disturbance occurs, for example, in the power supply.

2.6.1 FLIP-FLOP STORE

This is a feedback store. The early types used relays as binary components.

They are reliable and their circuit technique is simple; they require, however, a reaction time of several milliseconds and considerable power. For these reasons the relays have been replaced by electronic bistable circuits with tubes, transistors, magnetic cores and dielectric materials which have shorter switching times and to some extent a lower power consumption. A bistable system is necessary here for each bit.

Fig. 2.18 shows the block diagram of a four-place binary series register (for storing tetrads) consisting of the binary components M_0 to M_3 and the And-gates A_S or A_L with the delaying sections DS_S or DS_L . The delay in DS_S and DS_L corresponds to the pulse period τ of the number. In this way the pulses of all the places of the number supplied appear simultaneously at the inputs of the And-gates. If at this moment, i.e. when the last figure occurs at the input, the And-gates are opened via the second inputs through a pulse on the writing line, then the places of the number occupied by pulses ("L") will bring the appropriate bistable multivibrators out of the resting condition 0 into position L.

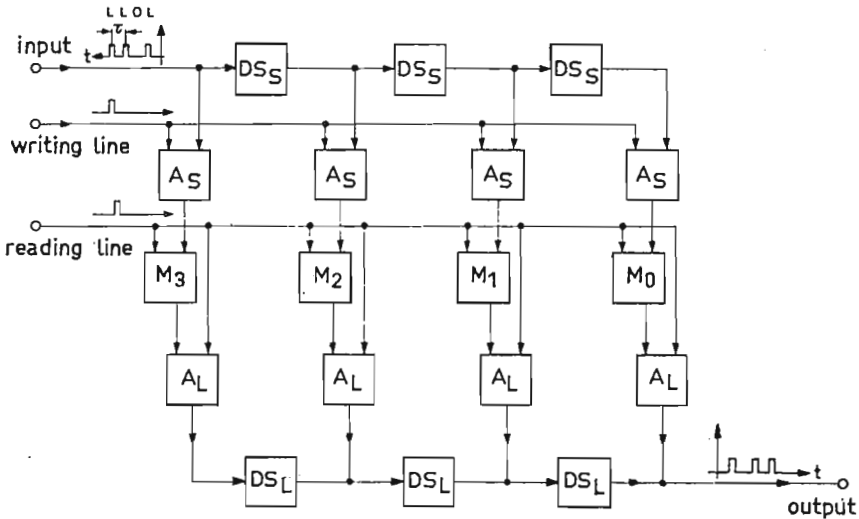


Fig. 2.18 Basic circuits of a binary series store

The outputs of the multivibrators are passed to a second series of And-gates A_L whose inputs in their turn feed a delay line suited to the one built up from the components DS_S . The reading is done through a pulse on the reading line. It opens gate A_L and reverses the multivibrators in position L back to the starting position 0. The output pulses produced give the stored

number LL0L, after a delay, at the output of the register. The register is thus cleared at the same time through the reading.

By using tubes with switching times of about $0.1 \mu\text{s}$, the access time lies below $1 \mu\text{s}$ which meets all needs. One disadvantage is the large amount of material required for greater storage capacities. The flip-flop store is therefore only used as the main store in small machines; on the other hand, it is becoming frequently used as a *register* (store for one word) in the arithmetical and control unit and as a buffer store in the input and output.

2.6.2 COUNTING CIRCUITS AS STORES [13]

If x input pulses are conveyed to a counter (see Section 2.4.3) in the zero position ($0 \leq x < B$), the counter then reaches position x in which it remains as long as required. It thus represents a store for digits in which one digit x is written through the introduction of a periodic sequence of x pulses.

All three of the storage principles mentioned can be realised, depending on the construction of the counter.

If a store of this kind is to be used in computers, it must also be possible to read the stored number electronically. This can be done statically by testing the places of the individual stages. If, however, we wish to refer back to the pulse series corresponding to the stored digit, the counter must be dynamically read. For that purpose we also need a frequency divider with the reduction ratio $1 : B$ (for which a counter can again be used) and a logical circuit composed of a bistable multivibrator and an And-gate. Fig. 2.19 shows as an example the block circuit diagram of a decade of a decimal counting store in which the number $x = 2$ is stored. With the reading of x , ten clock pulses are given to the input of the counter. This pulse series is simultaneously reduced $1 : 10$ in the frequency divider. After eight (generally

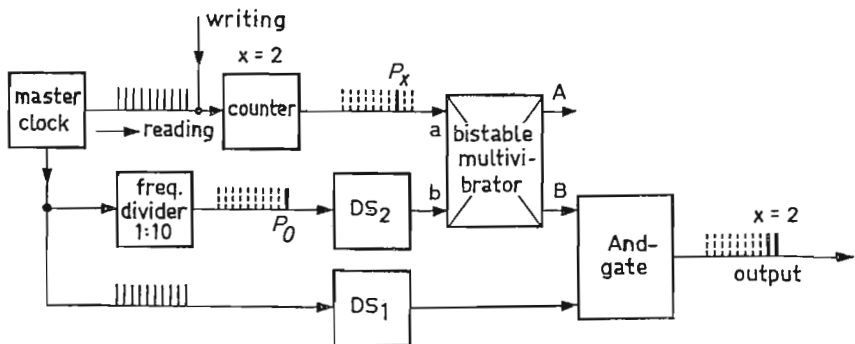


Fig. 2.19 Block diagram of a storage-counter decade

after $B - x$ pulses at the output the counter then supplies the pulse P_x , the frequency divider giving the output pulse P_0 after ten (B) pulses. The pulse P_x puts the multivibrator into the even condition (i.e. output B at low and output A at high voltage), and the pulse P_0 puts it into the odd condition. The And-gate is thus only opened from the eighth pulse to the tenth. Through a slight delay in the delaying component DS_1 only two clock pulses occur in the opening phase of the gate, so that the number of pulses corresponding to the stored digit x is yielded at the output. In order to prevent pulses P_x and P_0 occurring simultaneously at the inputs of the multivibrator in reading the digit 0, the output pulses of the divider must be held back to some extent in the delaying component DS_2 . After the reading the initially stored digit x is again in the counter so that the reading can be repeated periodically after each ten pulses.

The access time is determined by the limiting frequency f_{\max} of the counter; ten pulses are needed for reading, so that the access time for one decimal digit for example in a counter with 5 Mc/s limiting frequency amounts to about $2 \mu\text{s}$. Stores of this type are generally used as registers or intermediate stores, for instance in decimal arithmetical units in which clock, frequency divider and delay components can be the same for all decades. The outlay is too great for larger storage capacities.

2.6.3 DELAY STORE

Its principle is based on the delaying of pulse series; it thus acts as an energy store. If the number signals go over a delaying section in which the delay corresponds to a number period, each pulse of the initial signal then occurs at the output in the corresponding place of the subsequent number period. If we now take the output of the delay line over a pulse regenerating circuit to compensate the amplitude and phase distortion the pulses have undergone in the delaying section, and then back to the input, the number signal can circulate at liberty and thus remains stored. The delaying times needed in practice lie somewhere between $1 \mu\text{s}$ and 1ms . Times of this order can be achieved by tolerable geometrical dimensioning with electrical delay cables (low-pass with concentrated inductances and capacitances) or after conversion of the signals into mechanical oscillations through acoustic diffusion.

Fig. 2.20 shows the block diagram of a delay store. The pulses introduced through the Or-gate at input D circulate via the transmitter, delay section, receiver and pulse regenerating circuit.

The cycle is brought to an end through the blocking of the And-gate by a clearing signal at input A. If several numbers are to be stored, several parallel lines can be used, or the delay time can be extended over several

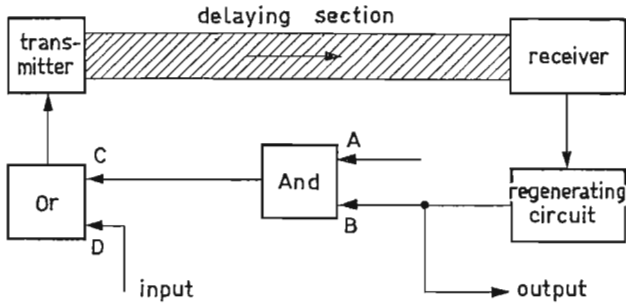


Fig. 2.20 Operation of a delay store

number periods, so that several numbers are accommodated one after another. In such cases delay stores are marked by their low cost. The most constant delay possible must be ensured to maintain the synchronism (for this reason, the delaying sections are mounted in thermostats). The stored information is only available when it arrives at the And-gate. The access time thus corresponds to the full cycle of the store.

Increased delay times can be achieved comparatively easily with acoustic delay sections. Fig. 2.21 shows the working method of a magnetostrictive delay section consisting of nickel wires. The current pulses of the transmitter circuit flow through a coil which encloses one end of the nickel wire. Because of the magnetostrictive effect these pulses are excited to mechanical longitudinal oscillations which are propagated in the wire with the velocity of sound. A receiver coil at the other end of the wire, pre-magnetised by a permanent magnet, undergoes magnetic changes of flow because of the change in permeability of the nickel wire brought about by magnetostrictive deformation. The induced voltage, amplified and regenerated, produces the output pulse. A store of this kind has the advantage that its delay time can easily be altered by moving the receiver coil.

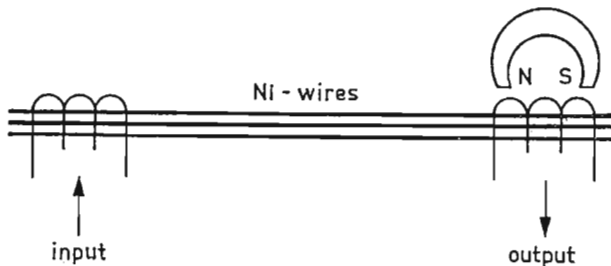


Fig. 2.21 Magnetostrictive delay section

Another type of acoustic delay store consists of a mercury reservoir, (50—100 cm long) in which the transmitter is an ultrasonic apparatus (quartz crystal) and the receiver is a transformer of the same kind. In comparison with the magnetostrictive delay line we here make use of an H.F. carrier (20 Mc/s) for diffusion. The number pulse is modulated to this. The damping amounts to about 5 db/ms.

Delay stores are well suited in series machines as inner stores for smaller storage capacities.

2.6.4 MAGNETIC STORES

Magnetic stores are typical examples of structural stores.

2.6.4.1 *Magnetic drum store* [42, 84]

This much used and reliable storage unit consists of a rotating drum (e.g. 15 cm diameter, 30 cm length, 6,000 rpm), which is covered with a thin magnetisable layer. The number pulses to be stored are written and read on this layer by means of magnetic heads according to the principle of magnetic recording; there is thus a rigid phase relation between the pulses and the drum's angle of rotation. Residual magnetic dipoles are produced in the storage layer through the writing currents in the coils of the magnetic heads. During reading these then induce electric voltages in the same head. There is no special clearing possibility; the current flow during writing is so strong that the corresponding storage component is brought to saturation independent of its condition. The pulse series frequency is limited to some 100 kc/s because of the inductivity of the magnetic heads. The storage layer has a thickness of about 10-20 μ and is made of electrolytic nickel or iron oxide with an organic binding agent.

The attainable storage density depends primarily on the distance of the magnetic heads from the drum and on the selected width of the track and amounts to a few bits per mm^2 up to 10 bits to the mm^2 .

Both the binary digits L and O can be written via positive and negative pulses, or the digit L can be written through a pulse of twice the magnitude on a premagnetised drum. Fig. 2.22 illustrates these two possibilities. The first line shows the binary number L0, the second line gives the corresponding writing pulse, the third the induced flow in the storage layer, the fourth the voltage induced in the magnetic head at the reading, the fifth line shows the pulse thus produced, and the last line the number L0 derived.

This process is known as the RZ-writing method ("return-to-zero") since here the magnetisation inside consecutive pulses of equal polarity

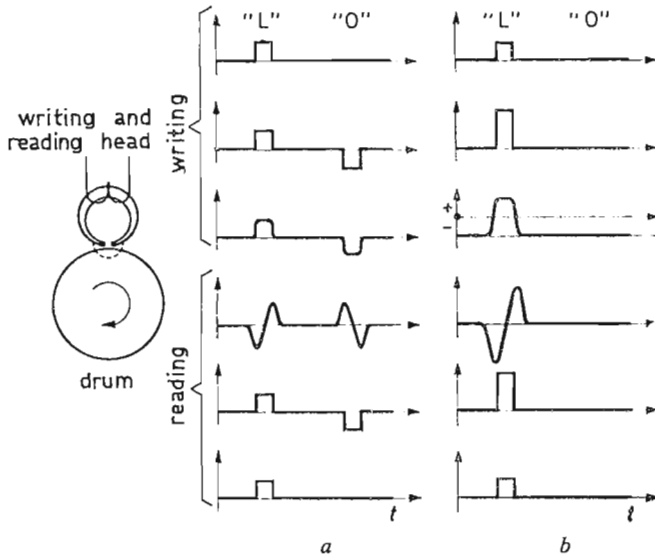


Fig. 2.22 a) Storage in both polarities
b) Storage with pre-magnetisation

also returns to zero. This method requires a bandwidth corresponding to the clock frequency $f\tau$.

With half the bandwidth $f\tau/2$ the so-called NRZ method answers the purpose. This is shown in Fig. 2.23. The reading voltage here (at the change of 0 and L) has half the clock frequency as basic frequency and triggers over a bistable multivibrator. Its output voltage goes to an And-gate at whose second input the clock frequency lies. The output of the And-gate then delivers the stored number.

In conclusion the clydonogram must be mentioned. Here L consists of a period of the sinusoidal voltage begun with the positive half wave and 0 is represented by a period of the sinusoidal voltage begun with the negative half wave. We obtain the stored number by rectification of the reading voltage. The bandwidth for the basic frequencies is between $f\tau/2$ and $f\tau$. The clydonogram has the advantage that no d.c. components need be transmitted.

Suitable writing and reading circuits are necessary to give correct coordination so that a number in the required cell of the drum, or a stored number, can easily be found again. Synchronism is obtained through the use of special timing tracks at one end of the drum. The synchronising signals are magnetically recorded on these. A particular storage cell can be traced through

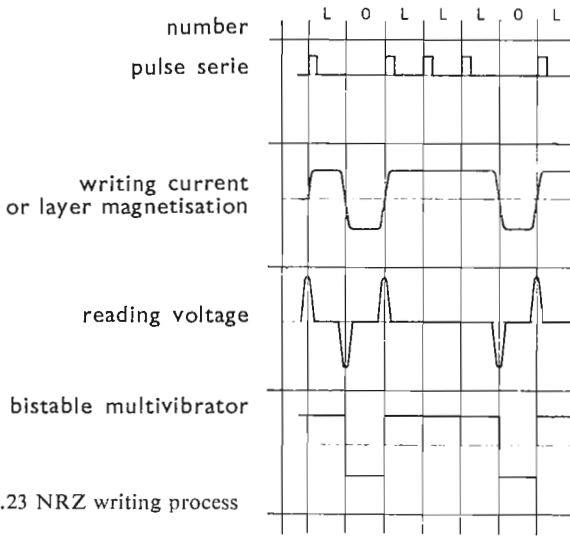


Fig. 2.23 NRZ writing process

the given address by counting the pulses coming from the timing tracks and comparing them with the address in an appropriate circuit. As an example, Fig. 2.24 shows the block diagram of a drum store for three-place addresses. The coincidence circuit only yields information at the moment when the value supplied by the counter agrees with the inserted address. This is the

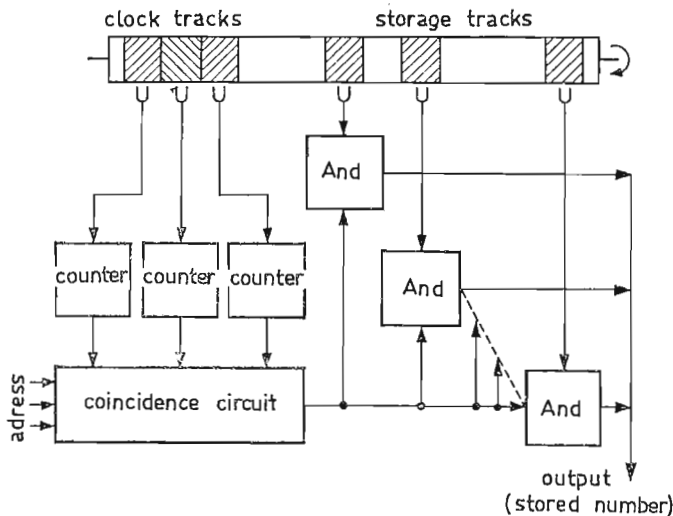


Fig. 2.24 Reading of the drum store

case when the desired storage cell is directly under the head of the track concerned so that it is possible to read the number above the And-gate fed by this head and the coincidence circuit. A drum store has several hundred heads in axial track spacing of a few tenths of a millimetre to about 2 mm, so that adjacent heads are displaced at the circumference for reasons of space. To obtain high storage density the heads must lie closely in front of the drum. Their distance from the storage layer is about 10 to 80 μ . This calls for great mechanical precision with high revolution figures (about 5,000 to 15,000 rpm). The access time on the average amounts to half a rotation. The capacity is determined by the size of the surface. Since the number of revolutions and the dimensions of the drum are limited for mechanical reasons, there is a simple relation between capacity and access time. We thus obtain favourable intermediate solutions for storage capacity and access time, e.g. 0.5×10^6 bit and 5 ms.

2.6.4.2 Magnetic core store

The magnetic remanence can be used with advantage for storage purposes through the homogeneous application of a suitable layer on to a drum or band; we can also make use of concentrated elements. For this reason we

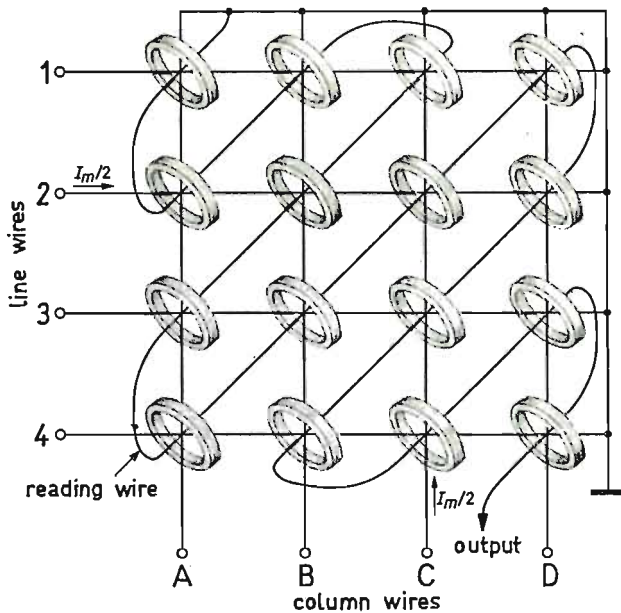


Fig. 2.25 Arrangement of ring cores in a matrix

mainly use small ring cores of certain ferrites. If the ring cores are arranged in matrix form (Fig. 2.25), we obtain a store in which through each pulse, a binary figure can be written on a selected line and column in the appropriate core, or can be read from it. The storage is based on the greatest possible rectangularity of the hysteresis loop of the ring cores in use, so that we simply utilise the conditions of positive and negative saturation remanence.

Fig. 2.26 shows the working method of storage with a hysteresis loop and a ferrite core. During writing, the core is excited by two windings, the line and column windings (generally consisting only of a wire passed through) that is to say, by pulses of such strength that their coincidence alone causes the reversion from one saturation condition to the other. Provided there is sufficient rectangularity, a pulse $I_m/2$ leaves the core practically uninfluenced. The positive remanence corresponds to the digit L, the negative to the digit 0. The excitation necessary to reverse the magnetisation is usually several hundred mA-turns.

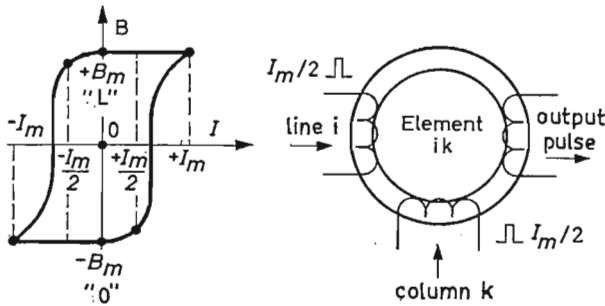


Fig. 2.26 Principle of the magnetic storage matrix

In series working only one line and column are selected at a time. With parallel writing, on the other hand, one line and all the columns which are to be engaged on this line with an L receive $+I_m/2$ pulses.

At the reading of the condition of an element ik , a negative pulse of the value $-I_m/2$ is given to each i th line and each k th column. If the ring core is in condition L, it reverses and supplies an output pulse in a third winding, the reading winding. Here the conditions of several cores must be read in periodic succession (series reading). We can also read the matrix in parallel, however, when, for example, a pulse of the value $-I_m$ is given in the i th line. Then all the cores of this line which are in positive remanence are reversed simultaneously and give output pulses in their column windings.

Thus no third winding is needed here, but the energy required for reading is undoubtedly greater. In series reading the reading wire is taken diagonally through the matrix as shown in Fig. 2.25. In this way we have two successive cores of one line and column passing through at a time in opposite directions, so that the disturbing pulses produced by the half pulses in the remaining components in the selected column and line are compensated.

Fig. 2.27 shows the block diagram of a simple writing and reading circuit for a series matrix with $n \times n$ elements. Here the choice of lines and columns is made through two ring counters Z and S (see Section 2.4.3.2). These are each composed of n bistable elements only one of which is in the "even" condition at a time. This condition is moved on by one element through each input pulse. Each element of the ring counter feeds a pair of And-gates but only the element in the even condition supplies the transmission voltage. The stored information is read in the following way: And-gate A_L is opened. The first clock pulse P brings both ring counters into position "1" and they, in their turn, open gates A_{1L} and A_{1L}' . At the same time, after a delay in DS , the pulse P arrives at all the line and column reading gates A_{1L} and A_{1L}' . It is only passed, however, by the gates for the first line and first column, so that the two driving stages T_{1L} and T_{1L}' each deliver a pulse $-I_m/2$ and the first core is read. The next P pulse brings the ring counter Z into position "2" (S remains in position "1") so that now the delayed pulse reads off the second element of the first column. In this way, all n elements of the first column are noted in succession. Pulse $n + 1$ brings ring counter Z back into position "1" and at the same time puts ring counter S into position "2" so that now all the cores of the second column can be read. After n^2 pulses the complete matrix has been read in this way successively column by column. The writing of fresh information proceeds accordingly since gate A_S is now opened, allowing the number pulses of the single lines and columns to pass to the writing gates A_{1S} and A_{1S}' . Their outputs feed the driving stages T_{1S} and T_{1S}' which then send positive pulses $I_m/2$ into the matrix.

Magnetic storage matrices are speedy (access time under $10 \mu s$) and are convenient for medium storage capacities and as buffer stores. Since we need $2n$ driving stages when we have n elements for each line and column in the simplest case, the greater the number of elements in the matrix, the more favourable is the number of driving stages required in relation to the capacity n^2 of the matrix. The number of driving stages can be reduced to $4/\sqrt{n}$ by special circuits (e.g. by using two switch core matrices [79]).

Instead of ring cores, the matrix can be composed of a flat perforated ferrite block through whose holes the line, column and reading wires are

threaded [16]. Finally, in place of the ring cores we can also use vaporised ferromagnetic alloys in thin layers.

With the simple working method of a core store as shown in Fig. 2.27,

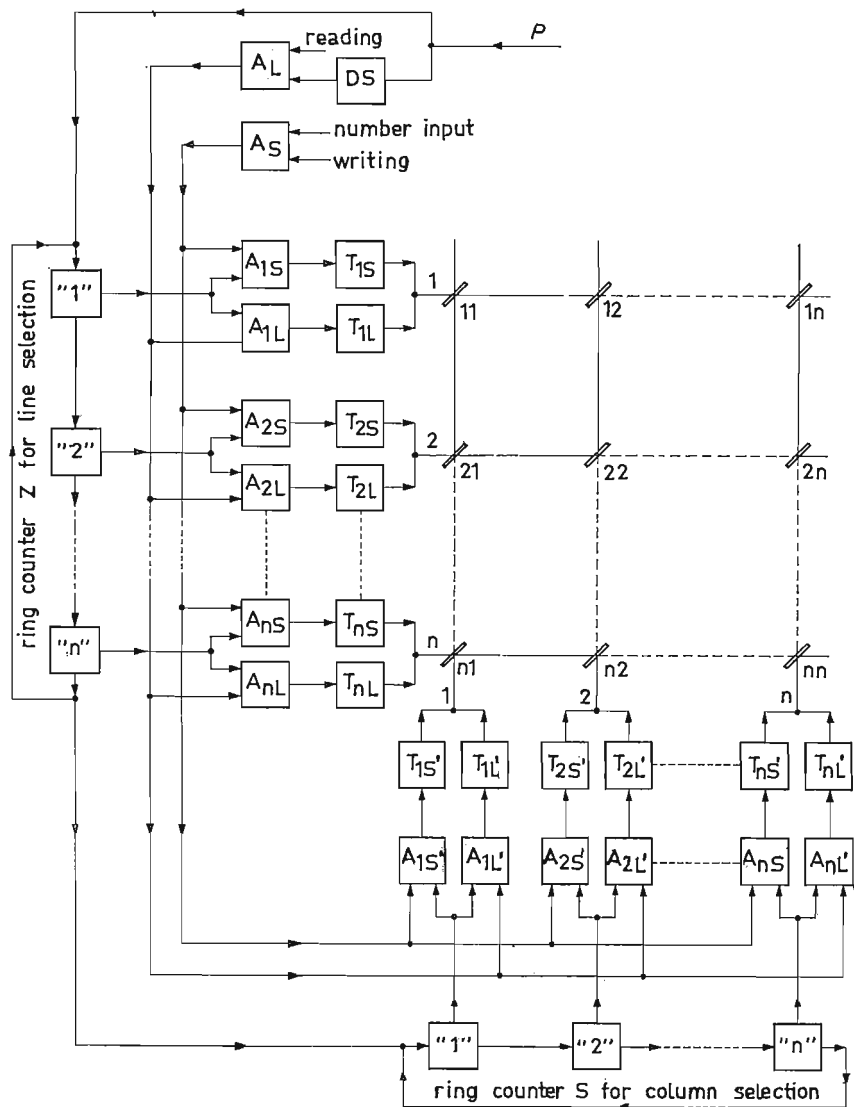


Fig. 2.27 Block circuit diagram of the writing and reading directions of a storage matrix (series operation)

the information is cleared with the reading. This is often not desirable and methods have therefore been developed by which the information is not cleared at the reading [17]: We can re-write the information read from the store through external circuits. In the transfluxor, a square loop ferrite core divided into two magnetically coupled circuits by an additional eccentric perforation, the information is stored in one circuit and then carried over into the other where it can be queried as often as desired. Another solution of the problem of reading without escape of information is based on the fact that with anisotropic materials, a change of magnetisation is partially reduced.

2.6.4.3 Other magnetic stores

Stores which require a large capacity but in which short access time is not of great importance can be constructed as magnetic tape storage units on the principle of magnetic tape apparatus. The tapes are usually continuous (e.g. 100 m) and are set in motion with a speed of several metres per second, through the summoning of a number, over low-inertia couplings. The information is written in several tracks side by side. Since the tapes are only moved when required, the magnetic heads can here be allowed to touch the tape and so, because of the small stray fields, greater storage density is obtained than with the drum store (in the direction of the track about 100 bit/cm). The access time is about 1 to 10 seconds depending on the band length and construction.

Another magnetic store of large capacity and proportionally less access time is the magnetic disc store of IBM [15]. It is composed of 50 discs of about 0.6 mm diameter which rotate one above the other on one axis at about 1,200 rpm, and one or more writing or reading heads which can be mechanically brought up to all the discs. One disc takes 100 tracks on each side. The capacity amounts to $35 \cdot 10^6$ bit with an average access time of 0.5 s.

2.6.4.4 Range of application of various magnetic stores

The question of production costs of the most important types of stores for definite access times and capacities is elucidated in Fig. 2.28. The necessary writing and reading circuits (with the use of transistors) are taken into account with the costs. For small capacities up to about 50 bits, the flip-flop store is the cheapest and quickest (access time 1 μ s); for medium capacities (50 to several thousand bits) the ferrite core store with an access time of about 10 μ s is recommended; with capacities of over 10^4 bits we use as an

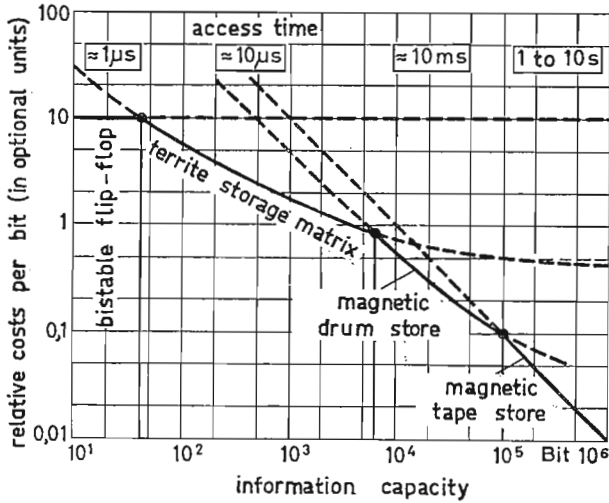


Fig. 2.28 Efficiency of various storage systems [9]

expedient the drum store with about 10 ms access time; and finally, with storage capacities above 10^5 we use the magnetic tape or magnetic disc store with access times between 0.5 and 10 s. We see that with the flip-flop store the costs increase in proportion to the capacity while for the magnetic stores the costs only rise by the third or fourth root of the information capacity.

The limits drawn in Fig. 2.28 are naturally not rigid but depend on the price level of the components required in each case. In view of the tendency of storage core and transistor prices to fall it might be possible, for example, to move the limit between core and drum stores to higher capacities.

2.6.5 FERRO-ELECTRIC STORAGE MATRICES [14, 66]

Ferro-electrics can also be used as storage media in analogy to the ferrites. With these the connection between field strength and electrical displacement is likewise in the form of a rectangular hysteresis loop. Such dielectrics are, for example, Seignette salt, the titanates of barium and strontium [18] and certain aluminium alloys [19].

Ferro-electric capacitors are constructed for stores of this type. The dielectric constant must be small in the saturation condition and large during reversal of polarity, as is obvious from the relation between the electrical displacement D and the exciting field strength E (Fig. 2.29). The circuit used

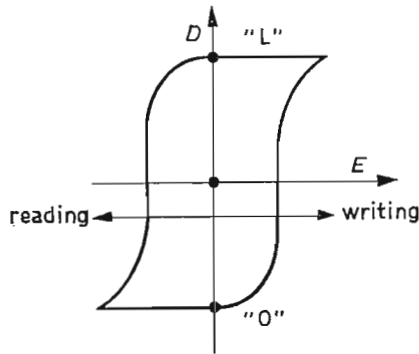


Fig. 2.29 Polarisation curve of a ferro-electric

here is shown in Fig. 2.30. The voltage division between the capacity C_S of the storage cell and the capacity C of the auxiliary capacitor is important. Writing is done by a positive pulse at input A which brings the dielectric into positive saturation (digit L) so that the output is short-circuited through the rectifier a. To read the stored condition a negative pulse is applied to input B which repolarises the dielectric into condition "0". ϵ_s is large during the reversal so that a negative pulse can develop at C and therefore at the output. On the other hand, if the cell is in condition "0" it has a very small ϵ_s for the reading pulse and the voltage division gives practically no output pulse at C . The two rectifiers b and c merely serve to avoid reactions on the preceding circuits.

We use the thinnest possible dielectrics (0.05 to 0.1 mm) so that we can manage with small control voltages. This keeps the heating of the store low at the same time. The maximum pulse series frequency lies at about 500 kc/s. At higher frequencies the rectangularity is impaired. There is, more-

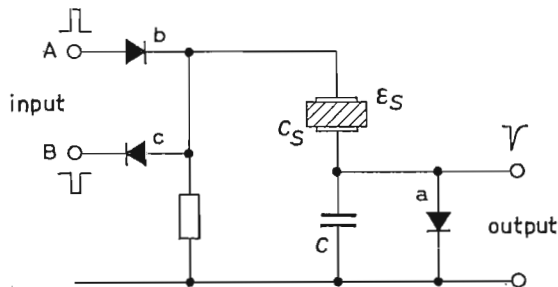


Fig. 2.30 Writing and reading circuit for a ferro-electric storage cell

over, greater dependence on temperature than with magnetic materials. In the practical construction of a ferro-electric storage matrix parallel metal strips are put on both sides of the dielectric in such a way that the strips on the two sides are perpendicular to each other, thus forming the lines and columns (Fig. 2.31). The individual storage cells then lie at the points of intersection of the perpendicular strips. In this way we get high storage density, about 500 bit/cm^2 . The pulse periods necessary for change of polarisation and therefore to some extent for the access time, are under $1 \mu\text{s}$. The saturation voltages fluctuate between 10 and 100 V so that only low current strengths are required in comparison with magnetic core stores.

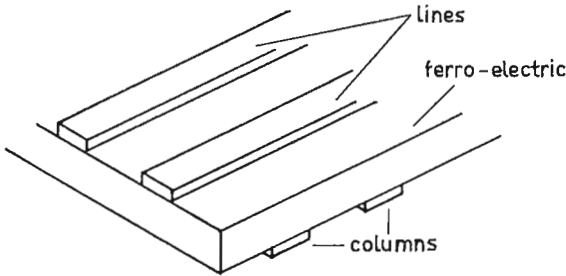


Fig. 2.31 Ferro-electric storage matrix

Ferro-electric storage units, however, do not hold the information indefinitely, but generally only for a few days depending on the ambient temperature.

2.7 Shift registers

The numbers to be processed are kept in the storage unit of the computer and can usually only be withdrawn one after the other. In the arithmetical unit, however, both operands are usually needed at the same time. An additional storage possibility is therefore needed through which one addend is detained until the second appears at the input of the arithmetic unit. Only then is it fed into the adding device. A store of this kind for the reception of one word is called a register. It can be composed of bistable components (see Section 2.6.1).

In many cases, however, single storing in the register is not sufficient. So the register, for instance with a binary series machine, must be able to take up the single digits of a number in periodic succession and deliver them again one after the other at its output independent of the moment of insertion. Furthermore, to carry out multiplication and division we must be able to

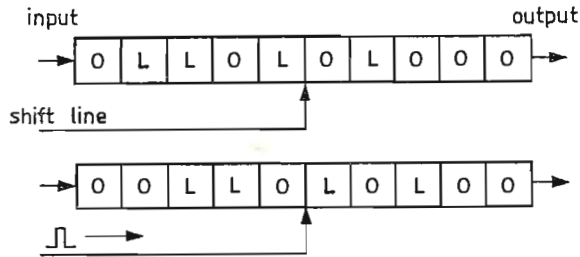


Fig. 2.32 Operation of a shift register

shift place values in the accumulator (see Section 2.3.1.3). These tasks are solved in a register whose contents, locked through a shift pulse, can be moved one place at a time. Fig. 2.32 shows the fundamental operation of this type of shift register. Through a pulse on the shift line the number stored in the upper position is moved one place, for example, to the right. When numbers are fed into the register, the contents already there must be shifted one place to the right through a shift pulse after each digit introduced, before the next place is passed to the input. As soon as the first place reaches the right end of the register, one digit appears at its output through each further shift pulse.

This kind of shift register can be made up from the basic circuits.

2.7.1 BINARY SHIFT REGISTER

Fig. 2.33 shows the block diagram of a shift register consisting of the bistable elements M_0 to M_3 and the delaying section DS. The bistable elements are at rest in the zero position, e.g. in the even condition. The coupling is such that only by switching over position "L" into position "0" is the following multivibrator released. The pulse series representing the number to be stored is fed in at the input and at the same time the shift line gets a pulse series from the master clock delayed by about half a pulse period. These shift pulses always bring about the zero position independent of the position of the individual multivibrators. Through the place first occupied by a L,

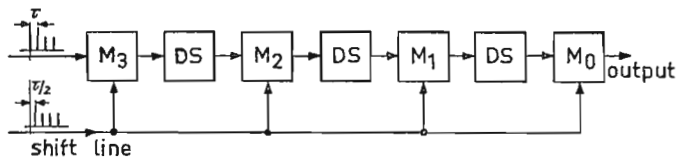


Fig. 2.33 Block diagram of a four-place binary shift register of the Woo type

M_3 is brought into the odd condition, i.e. into the L position. The succeeding shift pulse brings M_3 into position "0" through which a pulse is given at the output of M_3 ; this, however, may only appear at the input of M_2 after the conclusion of the shift pulse. This is achieved by an appropriate delay in DS. In this way, the number LOLL, for example, can be brought into the shift register in four strokes and is given up again at the output through four further shift pulses.

In addition to the dynamic storage in delay elements (Woo-Register [73]) the information between two stages can be stored statically in a separate bistable element. The block diagram of a shift register such as the Wang-Register [74] is shown in Fig. 2.34. Two bistable elements are required here for each binary number. The word is stored in the elements M_0 to M_3 and the elements m_0 to m_3 are in position "0". In order to shift the stored word one place to the right a shift pulse on line I brings the condition of the elements M_1 into the elements m_1 so that all the elements M_1 are brought into zero position. After a pulse on the shift line II the word is then in the elements M_0 to M_3 , i.e. shifted one place to the right. With series feeding each place thus needs three steps, one input pulse and two shift pulses.

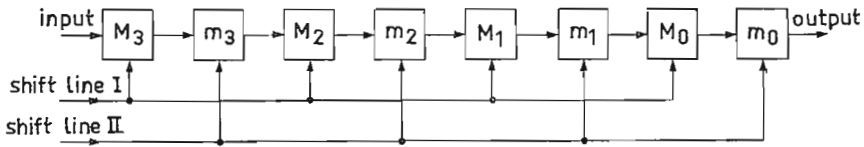


Fig. 2.34 Block diagram of a four-place binary shift register of the Wang type

Apart from the place method of addition of two numbers, the shift register is used in the arithmetic unit for multiplication and division as was described in Section 2.3.1; in this case each shift means a multiplication or division by the base.

In parallel working the shift register must be able to receive or give up all the places of a word simultaneously. Shift registers constructed in this way can then also serve as series-parallel transformers in which the single digits are fed in one after the other but yielded simultaneously from all stages of the register.

There are further possibilities of application of the shift register if we take the output back to the input. The stored word has then again reached its original position in an n -stage register after n or $2n$ shift pulses. The register now forms a dynamic store, used, for example, for magnetic switching circuits. If there is only one stage in condition "L", a pulse is yielded at the

output after every n or $2n$ pulses, the shift register acting as counter or as $1 : n$ or $1 : 2n$ reducer.

2.7.2 DECIMAL SHIFT REGISTER

Decimal registers are made up of decade counters. The place-value shifting, necessary in the accumulator for multiplication, for instance, then consists of transferring the contents of each decade into its adjacent decade. This can be done in two ways: We can either convey the single digits in series into the next places (in the form of pulse series) or we can transmit only the conditions of the single stages of the counter directly to the neighbouring decade. Extra measures are necessary in both cases to avoid collision between the individual decades.

Fig. 2.35 shows the decades of a shift register for series operation, for shifting place values to the right. Between each two decades there are auxiliary counters H in which the contents of the decades standing to the left are intermediately stored and which are all in zero position at the beginning of the shift. Shifting by one place is done in two steps: In the first, consisting of 10 pulses in line I, the digits a_i in the auxiliary counter H_i are carried over and the decades A_i brought into zero position. In the second step, through 10 pulses on shift line II, the digits a_i are moved from the auxiliary counters H_i into the decades A_{i-1} and the auxiliary counters again set to zero.

In detail, the place value shifting proceeds as follows: The multivibrators M_A and M_H supply, in the basic position, transmission voltage for the

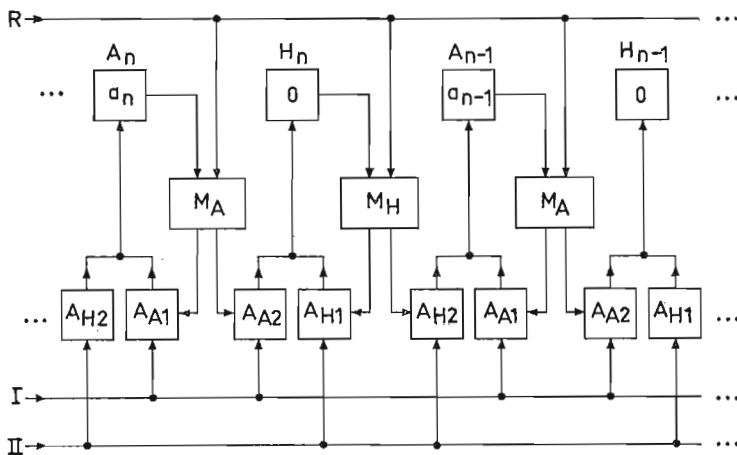


Fig. 2.35 Decimal shift register with series shift

gates A_{A1} and A_{H1} so that the clock pulses can flow from shift line I into decades A_1 . After each $10 - a_1$ pulses the carry-over pulses transpose the multivibrators so that now the gates A_{A2} retain the transmission voltage and the remaining a_1 pulses flow into the auxiliary decades H_1 while decades A_1 remain in the zero position. Ten further pulses on line II next flow via gates A_{H1} into the auxiliary counters H_1 whose carry-over pulses transpose the multivibrators M_H , and the remaining a_1 pulses flow into decades A_{1-1} .

After 20 pulses in all the shift is concluded. The multivibrators M_A and M_H are again switched back to their basic position through a pulse on line R.

This type of shift register demands a considerable amount of time for a place value shift (20 pulses) and needs twice the outlay in counting decades. The number of pulses can be reduced to two or even to one if we work in parallel. Here the single bistable stages of the counter are used twice. In one direction they are connected to a decade counter and in the other to a binary shift register.

We obtain a register of this type, e.g. from Fig. 2.34, by applying several binary registers one above the other and connecting their multivibrators

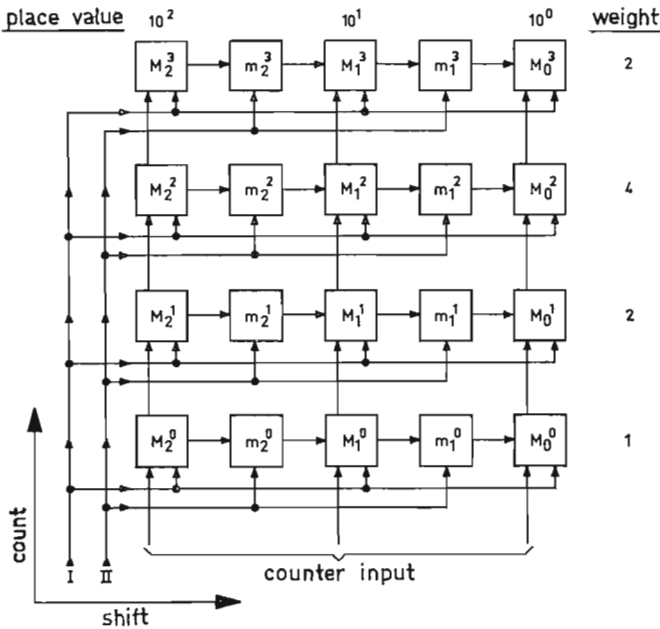


Fig. 2.36 Decimal shift register with parallel shift

M_0 to M_3 additionally to a decade counter. Fig. 2.36 shows the block diagram of a three-place shift register of this kind with tetrad-coded decade counters. The multivibrators M_i form the counters in the perpendicular direction, in the horizontal the shift registers, with static intermediate storage in the bistable elements m_i (Wang type). The shift proceeds in two steps: The first shift pulse on line I puts all the multivibrators M_i at zero; the output pulses thus produced engage the auxiliary stages m_i . The second shift pulse on line II brings the intermediate stages m_i to zero; their output pulses engage the next decade. Intermediate storage (in m_i) can be done in bistable multivibrators or in storage cores.

If we employ the Woo method in the horizontal direction, i.e. using a dynamic intermediate storage (see Fig. 2.33) we then only need one shift pulse and hence save expense. The delay stages DS can then be realised through RC sections.

2.8 The arithmetical unit

As we have seen in Section 2.3, every calculation is reduced to addition in the arithmetical unit. In subtraction this is done through the complement formation. Multiplication and division are resolved into addition or subtraction by means of a fixed programme in the control unit. Addition can be done in series working, i.e. single figures in succession, or in parallel, i.e. simultaneously next to each other. We propose to describe a binary arithmetic unit as an example of series working and a decimal one for parallel operation.

2.8.1 ELEMENTARY ADDING DEVICE

The elementary adding device necessary for the addition of two binary digits of one place of the set of digits must fulfil the rules of binary addition (2.14). It must also make use of the carry-over from the next place below. It therefore requires three inputs for the two addends and the resulting carry-over, and two outputs for the corresponding place of the total and the further carry-over to the next place. Fig. 2.37 shows this diagrammatically. Using the basic circuits it is now easy to put a circuit together which fulfils these conditions: All four totals in (2.14) are supplied by the Exclusive-or-gate (Fig. 2.4) while the carry-over is produced through the And-gate. To realise the rules (2.14) we thus only need to circuit an Exclusive-or-gate and an And-gate in parallel at the input, as Fig. 2.38 shows.

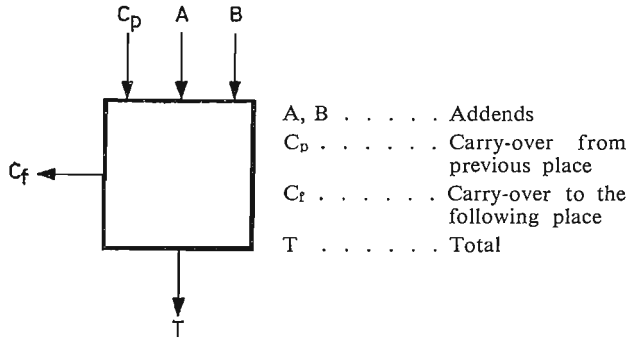


Fig. 2.37 Elementary adding device

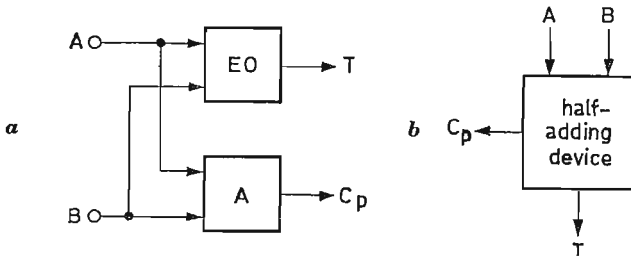


Fig. 2.38 Half adding device
 a) Composition from the basic circuits
 b) Schematic representation
 (EO . . . Exclusive Or-gate)

We then obtain from the addition of

- 0 + 0 : No information at EO or A: total and carry over 0
- 0 + L } : Information at EO, no information at A: total L, carry-over 0
- L + 0 }
- L + L : No information at EO, information at A: total 0, carry-over L

This arithmetical unit, however, is not complete since it does not take into account the carry-over from the preceding place. It is called a “half-adding device”. A complete adding device is obtained by connecting together two half-adding devices, as shown in Fig. 2.39. The carry-over of the preceding place is counted into the total in a second half-adding device and the carry-overs are added up. If the first half-adding device supplies a carry-over, its total is then 0 so that two carry-overs can never arrive at point Z at one time.

In order to use an adding device of this kind as the arithmetical unit of a machine, it must be supplemented by shift registers or delay lines.

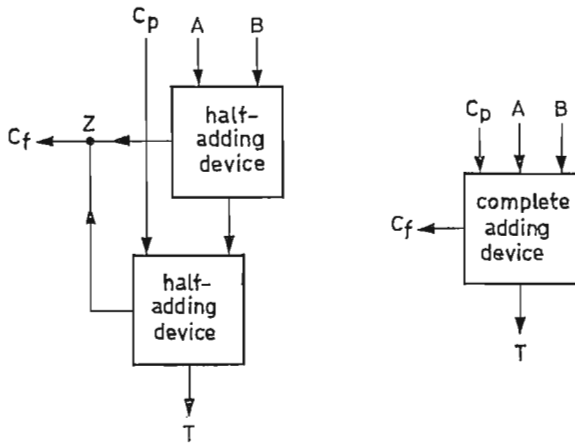


Fig. 2.39 Complete elementary adding device

2.8.2 BINARY SERIES ARITHMETICAL UNITS [11]

In series working the single places of each addend follow one another in periodic succession. For addition, therefore, it is sufficient to have a one-place adding device in which one place is added on after another beginning with the lowest. The carry-over C_f thus produced is taken to input C_p provided for the carry-over of the preceding place over a delaying section where it is retarded until the addends of the next place appear at the input. We thus obtain the series adding device by attaching a delaying section to the adding device, as in Fig. 2.39. Fig. 2.40 shows in diagram the addition of two binary numbers [11 and 13].

By using two shift registers we can now build up a completely binary adding device; its method of operation is illustrated with the help of the

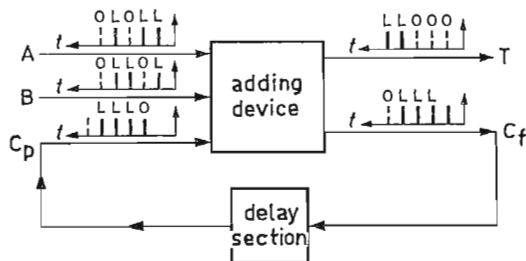
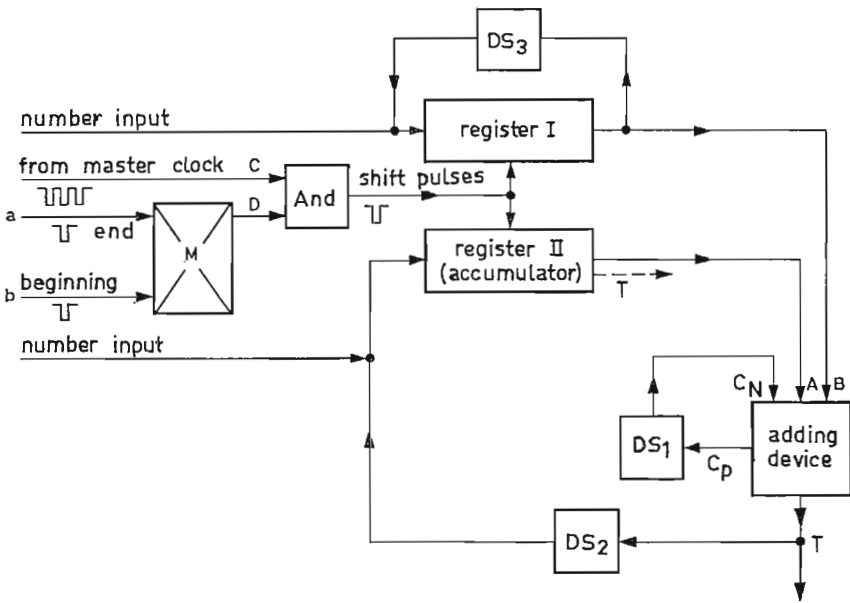


Fig. 2.40 Binary series addition: 01011 + 01101 = 11000

block circuit diagram in Fig. 2.41. First, both operands are conveyed successively to register I and register II, digit by digit.



2.41 Binary arithmetical unit with shift registers

The computation is started by a negative pulse at input *b* of the multivibrator *M*. This makes input *D* of the And-gate negative so that it now passes the clock pulses present at input *C* which operate on the shift line. Here each pulse from the two registers moves the digits two by two, one into input *A* and one into input *B* of the adding device. The total thus produced is conveyed to the input of register II after being delayed by half a shift period in *DS*₂. At the same time each digit given by register I returns again to the input of register I by the return line after delay in *DS*₃. After *N* shift pulses (*N* . . . number of places), the addition is checked through a negative pulse at input *a* of the multivibrator so that a positive voltage now reaches *D* and the gate yields no more shift pulses. We now have the total in register II, the accumulator, and the old addend in register I. The two numbers are then available for further operations or output.

In place of shift register II we can also use a delay store in the arithmetic unit (see Section 2.6.3). Here the numbers fed in circulate continuously with a cycle of at least one number period until they are cleared. Fig. 2.42 shows an arrangement of this kind. The first addend fed in via the Or-gate,

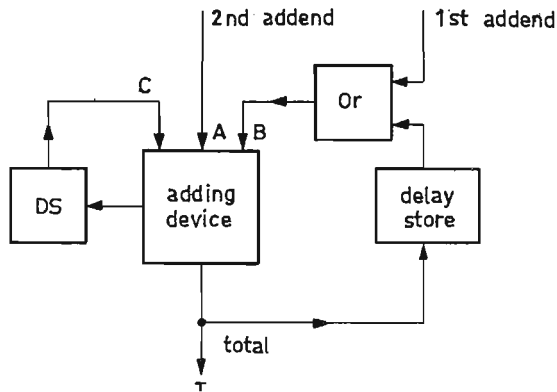


Fig. 2.42 Arithmetical unit with delay store

or the result of the previous computation, circulates continuously over the adding device and the delay store. The second addend, given at the correct moment at input A is then added to the stored number and the result remains stored or can be given up directly at T.

The arithmetical speed in the series arithmetical unit is determined by a given index figure through the pulse period τ of the master clock. For the addition of two N -place numbers we need time $N\tau$ for the purely arithmetical operation. Thus with $N = 40$ (about 12 decimal places) and 100 kc/s clock frequency, the time would be 0.4 ms. $N/2$ additions are required for a multiplication (compare Section 2.3.1.2) so that the multiplication of two 12-place decimal numbers needs about 8 ms.

2.8.3 ADDING DEVICES FOR BINARY CODED DECIMAL SYSTEMS

In computers which work with decimal numbers coded in binary tetrads, the four binary places of a decimal digit are treated in the arithmetical unit as if they were true binary digits. Addition can be done with the elementary adding device described, in which the addition of the four places of a tetrad is usually carried out in parallel. The pseudo-tetrads produced must be converted into true tetrads by appropriate rectification (see Section 2.2.3). The circuits required for this can be built up from the basic circuits [55].

In the addition of two biquinary coded decimal numbers, the quinary and the binary parts can be added separately. Here it is only necessary to ensure that the possible "inner carry-over" (a five) is taken into account. The quinary parts of the two addends can produce a total between 0 and 8, at the most 9 by the addition of the carry-over from the previous decimal

place. If the total lies between 5 and 9, the quinary part must be reduced by 5 by giving the inner carry-over to the binary part of the total. "Fives" (L0) can thus occur here from three different places: from the binary parts of the addends and from the carry-over of the quinary part of the total. The addition of the binary parts and the production of the carry-over to the next decimal place correspond to an ordinary binary addition of two two-place addends, taking into consideration the carry-over from the previous decimal place. It can thus be carried out in an addition circuit according to Fig. 2.39. The addition of the quinary part can be done likewise through a suitable combination of a series of And-and Or-gates, but it requires more outlay [55].

2.8.4 DECIMAL MULTIPLICATION

So that we can refer back to binary information in the uncoded decimal system, we reduce addition to counting by representing each decimal digit through a corresponding number of pulses. The arithmetical unit is then composed in essential of decimal counters (compare Section 2.6.2). To add two digits x and y with one counter, we only need to take the two digits x and y to the counter in the form of a suitable pulse series. Its contents then correspond to the total $x + y$.

Multiplication can be done in two ways according to our explanations in Section 2.3.1.2: First we can form all the partial products of both factors (one after another or several simultaneously) (see Equation 2.8). We can also multiply the entire multiplicands consecutively by the single digits of the multiplier (see Equation 2.9). In both cases we have to make sure that the place values are correct in totalling up the products, so we either arrange the accumulator as a shift register or, through a switch-over, allow the single partial products to flow into the accumulator in correct place values. There are thus four possibilities for a multiplying device consisting of counters: Totalling up the partial products in series or in parallel on the one hand, place value switch-over or the shift register on the other.

In each case the multiplication is carried out in conformity with the principle of multiplying two one-place factors as shown in Fig. 2.43: This type of multiplication device consists in principle of the series circuit of two storage-counter decades (see Section 2.6.2). Each 10 pulses at the input of the decade with the content x_1 give x_1 pulses at their output; 100 input pulses therefore give $10x_1$ output pulses. On the other hand, 10 pulses at the storage decade with the content y_1 give y_1 pulses at its output, thus $10x_1$ input pulses, altogether x_1y_1 output pulses. 100 pulses at the input of the multiplier register in this way yield the partial product x_1y_1 in the accumulator.

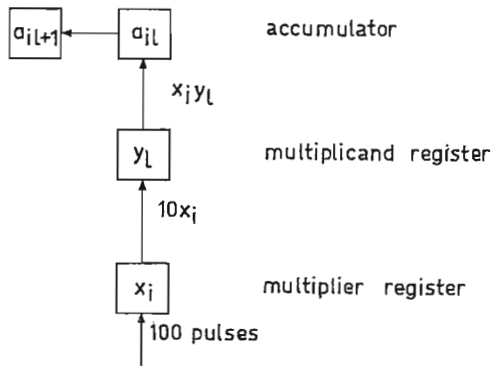


Fig. 2.43 One-place multiplication circuit

2.8.4.1 Series multiplication with place switching

By placing N such multiplication stages in adjacent rows and arranging correct place values in the accumulator, we can build up a multiplication device in a simple manner as Fig. 2.44 shows in an example for three places.

The product of the two three-place numbers

$$x = x_2 \times 10^2 + x_1 \times 10^1 + x_0 \times 10^0$$

$$y = y_2 \times 10^2 + y_1 \times 10^1 + y_0 \times 10^0$$

can be composed of the following 9 partial products:

Schritt	10^4	10^3	10^2	10^1	10^0
1					$x_0 y_0$
2				$x_0 y_1$	
3				$x_1 y_0$	
4			$x_0 y_2$		
5			$x_1 y_1$		
6			$x_2 y_0$		
7		$x_1 y_2$			
8		$x_2 y_1$			
9	$x_2 y_2$				

The arithmetical unit consists of a three-place register I for the multiplier, a three-place register II for the multiplicands and a six-place accumulator for the product. The selection of the single partial products is controlled by a series of And-gates through the nine stages of a ring counter which

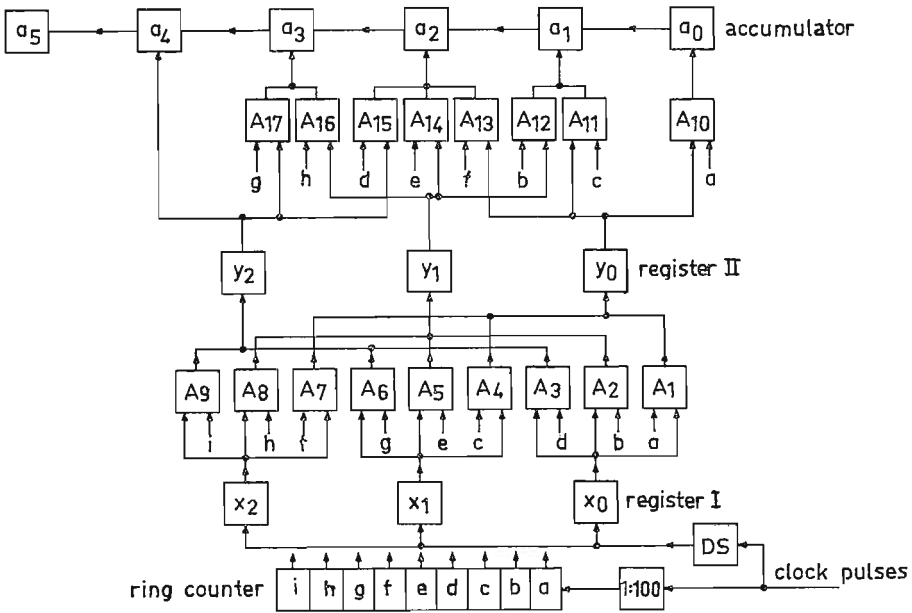


Fig. 2.44 Series arithmetical unit with switch-over of places

after every 100 clock pulses switches forward by one place. The ring counter is in position a in the basic circuit. The gates A_1 and A_{10} are open for the first 100 clock pulses; x_0y_0 pulses flow from the multiplicand register into place a_0 of the accumulator. A carry-over produced here goes on into the next place a_1 . The 101st pulse brings the ring counter into position b, and now the partial product x_0y_1 runs into place a_1 of the accumulator. (The delaying stage DS is intermediately connected so that the ring counter has already switched forward before the 101st pulse arrives at the multiplicand register.) In this way the multiplication is concluded after 900 pulses in all.

A computation of this kind is relatively slow. It needs N^2 clock pulses for one multiplication (i.e. about 130 ms for 8×8 places at 50 kc/s clock frequency). On the other hand, no outlay is required here for intermediate storage and the passing on of the carry-over produced in the accumulator.

2.8.4.2 Parallel arithmetical unit with place switch

We now proceed according to Equation 2.9. The product of two three-place numbers is then composed of three steps:

Step	A_4	A_3	A_2	A_1	A_0
1					$(y_2 \times 10^2 + y_1 \times 10^1 + y_0 \times 10^0)x_0$
2					$(y_2 \times 10^2 + y_1 \times 10^1 + y_0 \times 10^0)x_1 \times 10^1$
3					$(y_2 \times 10^2 + y_1 \times 10^1 + y_0 \times 10^0)x_2 \times 10^2$

Here the entire multiplicand thus flows x_1 times into the accumulator so that intermediate storage is now necessary for the carry-over in the accumulator. Correct place value arrangement is achieved through a switch-over via the And-gates. Fig. 2.45 shows the block circuit diagram of a multiplying device of this type. It is composed of the three-place register for the multiplier x , the three-place register for the multiplicand y and the six-place accumulator for totalling up and storing the product.

Over and above this, three And-gates are needed to select the individual partial products and nine And-gates to transport them into the accumulator; these are controlled by the respective position of a three-stage ring counter I. Finally the ring counter II takes care of the passing on of the carry-over pulses in the accumulator. The single stages of the register are again composed of storage decades which can be read in series (see Fig. 2.19).

In detail, multiplication goes as follows: Ring counter I is in position a at the start of the computation and the multivibrator M has opened gate A .

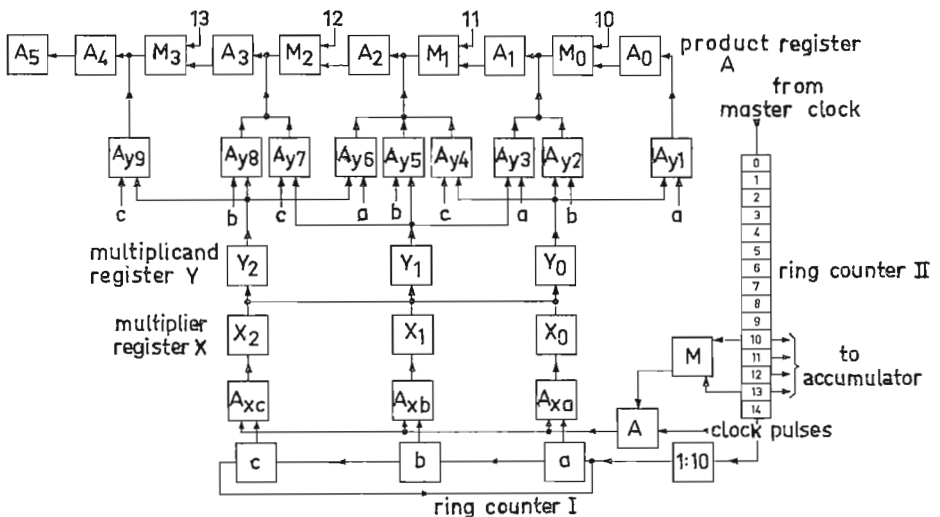


Fig. 2.45 Parallel multiplication device with switch-over of places

Of the gates A_{xi} , only A_{xa} passes the clock pulses, while of gates A_{y1} , A_{y1} , A_{y3} and A_{y6} are opened for the pulses coming from registers X. The clock pulses thus flow via the gates A and A_{xa} into place x_0 of the multiplier register. The carry-over produced in the accumulator by the totalling is intermediately stored in the bistable multivibrators M_0 to M_3 which are read after each 10 pulses. After 10 pulses the multivibrator M is switched over through the ring counter II and gate A is blocked. The four succeeding clock pulses switch the multivibrators M_0 to M_3 in consecutive order back to the basic position, through which the carry-over is passed on into the next accumulator place. The 13th pulse opens A again so that 10 further pulses flow towards x_0 . After 10×15 pulses in all, the first partial product is in the accumulator. The clock pulse which now follows switches the ring counter I into position b, initiating the formation of the second partial product. After 3×150 pulses altogether the multiplication is complete.

With this method we usually need $150 N$ clock pulses for multiplication with an N -place factor. The index number of the multiplicand has no effect on the arithmetical speed.

2.8.4.3 Parallel arithmetical unit with shift registers

Here we also proceed in accordance with Equation 2.9 but, starting with the lowest figure of x , we allow the partial products to run into the individual places of the accumulator without switching over. The correct place value totalling of x_1y is thus obtained by shifting the contents of the accumulator one place to the right after each partial step. The accumulator has therefore to be constructed as a shift register (see Section 2.7.2).

The principle of this type of arithmetic unit is shown in Fig. 2.46. It consists of an N -place register I for the reception of the multiplicand y , an $N + 1$ -place accumulator for the totalling of y and an N -place register II for the multiplier x and for the last N places of the product. Accumulator and register II are constructed as shift registers and are wired in series. The multiplication is carried out as follows: The number of totals of the multiplicand y in the accumulator is controlled by the last place of the multiplier x situated in R_0 . After each 10 pulses the digit in R_0 is reduced by one unit via line (1) and the carry-over from the accumulator induced through line (2) is passed on. This is repeated until the contents of R_0 reach zero, x_0 times in all. In this way, $10 x_0$ pulses flow into register I over line 3, that is to say, the multiplicand would be totalled x_0 times in the accumulator. Now the contents of the accumulator and of register II are shifted one place to the right (line 4) so that x_1 is now in R_0 and the formation of the second partial product can begin. As a result of the pre-

obtain the ten-complement we merely need to switch the multivibrator excited by the counter and the 1 : 10 reduced pulse series (Fig. 2.19) into the other place before reading. Then the And-gate stays open until the arrival of P_x . It thus passes $10 - x$ pulses, the complement. P_0 again opens the gate. To obtain the nine-complement in this way, the first pulse is suppressed when the counter is read.

2.9 The control unit

The control unit has the task of transforming the instructions supplied to the machine in coded form consecutively into suitable control voltages which then ensure the correct progress of the arithmetical process in the remaining parts of the computer. The number traffic is thus controlled between the individual main parts and a definite arithmetical operation with definite numbers can be accomplished.

Instructions and numbers are deposited in the cells of the main store under a specific address. At the beginning of a new step in the course of the programme, the appropriate instruction is withdrawn from storage and held in the control unit in an auxiliary store until the instruction is carried out. Suitable decoding circuits then convert the instruction into the control voltages which arrange the appropriate places in the computer to fulfil the instruction. The control unit also contains a number of gates and delay elements and in some cases a small arithmetical unit which serves as a calculator for the address of the following instruction. A speedier store uses an auxiliary store in the control unit; this holds the written information ready in the shape of static voltages (e.g. a flip-flop store). In the simplest case with a single address machine (see Section 2.1.3) this information is made up of two parts, the operation part and the address part which should both be binary coded. After introduction into the auxiliary store, the first part thus represents the digits of the operation part, the second the address of the instruction to be carried out. The capacity of the auxiliary store must be sufficient to receive one instruction word.

2.9.1 INSTRUCTION DECODER

Operation and address parts are converted into the control voltages in suitable separate coincidence circuits, the so-called decoders. For instance, to decode 16 possible different operations in a four place operation part, we need 16 And-gates each with four inputs, as is shown in Fig. 2.47. These inputs are fed by the two outputs of four elements of the flip-flop store so that all 16 possible combinations occur. Then each operational instruction

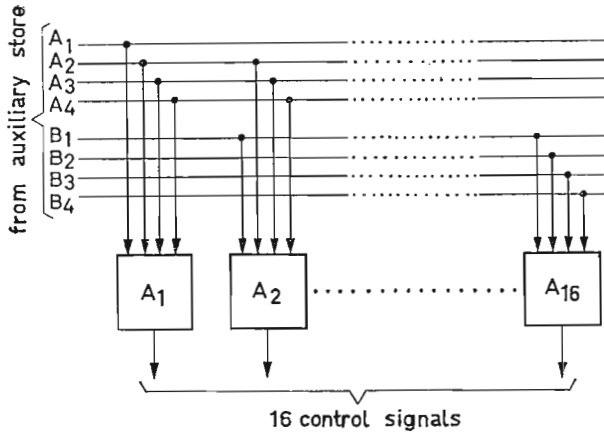


Fig. 2.47 Block diagram of the decoder for a four-place operation instruction

comes up against only one gate at a time which supplies it with information and thus with the particular control signal to the required place in the machine. An equally suitable decoder is necessary for the decoding of the address part of the instruction. By the appropriate gate this addresses the storage cell into which the required number is to be delivered.

2.9.2 CONTROL UNIT OF A ONE-ADDRESS MACHINE [11]

Fig. 2.48 shows a diagram of the construction of a simple control unit. The instruction series should be lodged in consecutive cells of the main store and the individual cells numbered in running order. As well as the auxiliary store and the two decoders, there is also the register for the instruction address in which, during one arithmetical step, the instruction for the next step is stored. Each arithmetical step is now made up of the switch-phase and the performance-phase, both of which are again divided into part-phases. Each part-phase corresponds in general to a number period of the master clock:

1. During the first number period of the switch-phase, one unit for the formation of the address of the following instruction is added in the adding device to the address circulating in the instruction-address store, (delay store) by operating the And-gate A_1 . The new address remains stored here for the next switch-phase and at the same time goes into the address part of the auxiliary store via the Or-gate O through operating gate A_2 .

2. In the next number period the address in the auxiliary store is decoded in the address decoder and the corresponding gate A_{3i} opened so that

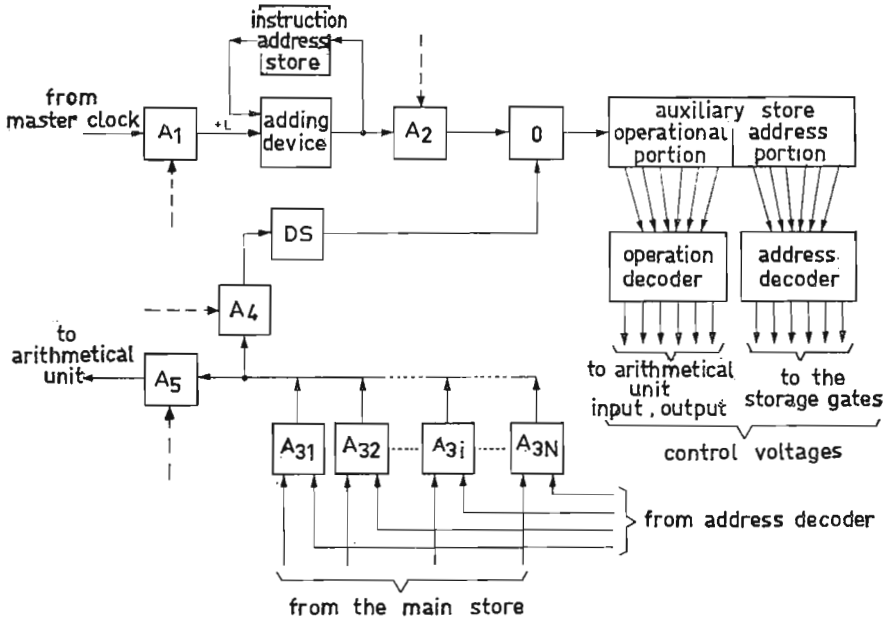


Fig. 2.48 Block diagram of a one-address control unit

the instruction word stored in the chosen cell i flows into the delay element DS by operating gate A_4 . It is detained here until the old address in the auxiliary store can be cleared.

3. In the next number period the control voltage for transmitting the necessary operands into the arithmetical unit, e.g. from a specific cell via gate A_5 , is generated in the address decoder and the control voltage for the required arithmetical operation is obtained in the operation decoder which the arithmetical unit sets accordingly.

The actual arithmetical operation is then concluded in the execution phase. The inputs of the gates, shown dotted, are operated by the master clock so that they are gated at the correct moment by frequency dividers or delay lines.

This description of the control unit only represents a rough approximation of its actual working methods, since many details have been omitted.

CHAPTER 3

COMPONENTS FOR DIGITAL COMPUTERS

Typical components for digital computers are vacuum tubes, gasfilled tubes, semiconductor diodes, transistors and magnetic cores with rectangular hysteresis loops. Many of the basic circuits described can be composed of these components, and the decision as to which components to use for a particular purpose often needs careful consideration including the comparison of their properties one against the other. The important points in judging computer components are reliability, durability and their minimum switching time, that is the transition time between two stable conditions. In addition, the question of extra switching equipment in the circuit, the energy consumption and the space needed, as well as the price, are all important. On the grounds of working reliability, we aim, above all, at the simplest possible circuits (with few resistances and capacitors). The energy taken up is converted into heat and must be discharged again through suitable cooling. Since the technique of the printed circuit is becoming increasingly used, it is also important that the components should be suitable for inclusion in printed wiring, their size being of the utmost significance.

With the useful *vacuum tubes* (single and multi-grid tubes) we attain switching times of about 10^{-7} s. Their reliability and durability have been substantially increased in recent years by the construction of special long-life tubes which has considerably improved the working reliability of digital computers. The tubes undoubtedly develop large amounts of heat as a result of their great energy consumption (heat and electrode leakage capacitance) and require a relatively large space. For this reason there has been a tendency in recent years to replace vacuum tubes where possible by simpler and smaller components. *Cold cathode trigger tubes* have grown in importance lately for switching purposes. These, as is known, are small gasfilled tubes with a cold cathode which can be ignited by a starter electrode. By the technique of molybdenum atomisation used in these tubes, the durability factor is substantial and the ignition and burning voltages have a high constancy during operation. Trigger tubes need no heater supply and do not deteriorate when no current is flowing. Finally, in many cases

they allow a particularly simple circuit construction. Naturally, there is no possibility of short switching times with gas discharge tubes of this kind. They can make use of a pulse series frequency of several kc/s. Their use in computer technique is therefore limited to circuits in which speed is not of prime importance, as for certain storage purposes, switching work, or counting and arithmetical circuits in simple office calculators with an electronic arithmetical unit. It is often an advantage here that the trigger tube indicates its condition by means of its luminous discharge. It should be mentioned that stabiliser tubes can also be used in computers. Gates, bistable circuits, counters and registers can be constructed with them [56].

Semiconductor diodes and transistors have also acquired great significance in computer construction, as in many other spheres of electronics. Because of their long life and reliability, favourable electrical properties, small energy consumption and low demand for space, the semiconductor devices have ousted tubes in most modern machines. In some cases the comparatively low maximum working temperature, the dependence on temperature, and limited blocking resistance are a disadvantage to be considered. Semiconductor diodes assist in the construction of logical and coding circuits and are also used in combination with tubes, transistors and ferrite cores. Here we make a distinction between low and high resistance fields of application. The germanium point-contact diodes usually meet the demands in high resistance use, as for example, in connection with tubes and transistors in order to maintain a certain potential with which to pass or block pulses of definite polarity. For circuits which need smaller transmission resistances, e.g. when used with square loop ferrites, the gold-bonded diodes are recommended. Their transmission resistance is less than 5Ω at a voltage drop of 1 V. Their use in logical circuits depends ultimately on the greatest possible ratio of blocking resistance to transmission resistance. A third type of semiconductor diode, the zener diode [57, 69] is also used in computer construction. This operates as a junction diode composed of a silicon monocrystal with an aluminium wire inserted; its working point lies in the blocking range in contrast to the usual diodes. The zener diode no longer functions from a certain blocking voltage onwards; the characteristic curve suddenly drops steeply to large blocking currents. Owing to its construction the value of this "zener voltage" can be selected within wide limits (from 3 V upwards). Before reaching this voltage, zener diodes have very high resistances (at 25°C , 10^7 to $10^9 \Omega$); on reaching the zener range they then have a differential resistance of only about 10Ω . This low value and the sharp transition between the two

ranges make the zener diodes very suitable for limiting and maintaining voltages, especially in connection with transistor circuits.

As a rule, only junction diodes are used at present in computer circuits, chiefly on account of their reliability, although there are a number of transistors which can form a bistable element on their own account, as for example, the point-contact transistor, the double-base diode [60], the four-layer diode [61] and the Salow-Münch transistor tetrode [62]. In recent years, transistor circuits built up in more or less close analogy to tube circuits have been increasingly developed as logical circuits, counter, writing and reading circuits for magnetic core stores. The *junction transistor* in grounded emitter circuit comes very near to an ideal circuit and with its small energy consumption, low feed voltage and simple handling, is the ideal component for computers. Because of its small size it is also well suited to printed wiring. The energy demand of a computer constructed with transistors amounts to only about 5 to 10% of the consumption of a corresponding equipment equipped with tubes. The transistor is, in principle, replacing the tube in most cases in the circuits used in computers. There are difficulties in the need for low tolerances, the dependence on temperature, and in some applications, in the demand for short switching times, with large currents and voltages.

The first computer built with transistors, the TRADIC, contained 700 transistors and 1100 diodes [22]. The switching times lie around 1 μ s. In working with this machine, special value has to be attached to the constancy of the ambient temperature. The point contact transistor 2N67 was used since it worked more quickly than the junction transistors at that time (1953). Up-to-date junction transistors, however, switch at greater speed, are more stable and have lower production leakages, so that with new developments, point contact transistors are no longer used. In the years 1954/55, the IBM machine 604 was changed over to junction transistors. This medium 13-place machine which works in the decimal system for commercial uses (60 plug-in programme steps), contains 2200 transistors and 3600 semiconductor diodes. The germanium junction transistors used have a limiting frequency between 0.7 and 1 Mc/s and are chiefly operated with a current amplification somewhere between 40 and 90, in the emitter circuit, so that many times the possibilities given by complementary transistors can be utilised. The clock frequency amounts to 50 kc/s, 0.5 to 30 ms being needed for each computing step. The experience gained with this machine — particularly in view of the high durability — pointed to the great importance of transistors in future computers. Another transistor computer was developed in 1956 by the Bell Telephone

Laboratory [28]. It contains 5,000 galvanically coupled transistors, works in the binary system (18 binary places) and needs 0.04 ms for an addition and 0.4 ms for a multiplication. A further range of computers with transistors is at present in production.

A further important component for electronic digital computers is the core of magnetic material having a rectangular hysteresis loop, made in particular of nickel-iron alloys and above all, the ferrites. These are generally used in magnetic storage matrices in the shape of small ring cores. (The computer JOHNNIAC, for example, contains 170,000 ferrite cores for storage purposes [24]). Materials with rectangular hysteresis loops are increasingly replacing tubes and transistors in other switching tasks, as in logical circuits, in ring counters and shift registers [63, 65, 67], in which the maximum switching frequency is somewhere between 100 kc/s and 1 Mc/s. Thus, if rectangular materials are also used in magnetic amplifiers, a computer can be constructed which (apart from resistors and capacitors) contains only square loop cores and semiconductor diodes. The arithmetical speed of a machine constructed on this basis [64] corresponds to that of the tube machine UNIVAC I. The ferrite core has such great durability that up to now no data are available for it. In the stationary condition they consume no energy and the generation of heat is thus minimal. They are also very small. The technique of printed wiring can be employed when they are used in storage matrices [40]. Currents between 200 and 1,000 mA are needed to reverse the magnetisation of ring cores, so specially developed rapid-action components must be used for this purpose. It is a drawback for some uses that the condition of the usual ferrite rings cannot be recognised directly but can only be examined electrically so that the information thus obtained is only dynamic.

As well as the ferrites with rectangular hysteresis loops, soft magnetic materials have some importance for magnetic heads in drum stores. The heads used here are marked, in comparison with those used in sound recording, by a comparatively large air gap, determined by the mechanics of the drum. Since the pulse series frequencies in drum stores lie in the 100 kc/s range, the heads must also be adapted to transmit high frequencies. It is obvious that for such requirements, heads made of ferrite are superior to the usual ones made of nickel-iron alloys [25].

The most important components will be briefly described in the following sections without going too closely into physical fundamentals and detailed technical data. Instead, only those viewpoints are stressed which are important for use in computers and which contribute to the understanding of information contained in technical data sheets.

3.1. Vacuum tubes

The use of tubes in digital computers differs from most other fields of application chiefly in the fact that only blocked and open-circuited tubes are used as stationary conditions. In view of the large number of tubes fitted in computers, special value must be attached to their great reliability and durability. Furthermore, for working reliability it is necessary for the individual tubes of a type to show low tolerances in their two stable conditions. Finally, with a great number of tubes, the requirements of heat capacity are important since these help to decide the heating of the equipment. A suitable ratio of anode current to heat capacity must therefore be aimed at. On the other hand, in computer use there are no demands with regard to noise, hum and microphony of the tubes.

These particular conditions have led to special developments in tubes for digital computers whose essential characteristics are summarised as follows:

1. High reliability
2. Long working life
3. Small tolerance of blocking voltage at the control grid and of anode current for zero grid potential
4. Little inclination towards intermediate layer formation
5. Low blocking voltage
6. Low tube capacitances
7. Small internal resistance of open circuited tubes
8. Favourable ratio of anode current to heat capacity
9. Low demand for space

3.1.1 THE TRIODE AS A SWITCH

High arithmetical speed demands quick opening and shutting of the tubes. The switching times are limited above all by the recharging of the harmful parallel capacitances effective at the anode, and correspond approximately to the rise or fall time of the change of anode voltage when switching the tube. The harmful parallel capacitance at the anode consists in this case of the output capacitance, the switch capacitance and the capacitance of the connected consumer (e.g. the effective input capacitance of the next tube). In practice the values for the parallel capacitance C_p lie between 20 and 50 pF, according to the components used and the circuit.

The two static conditions of the tube are shown in Fig. 3.1 in the I_a/V_a characteristic curve. In the in-position at point X , the tube is opened by the grid voltage $V_g \approx 0$. The maximum anode current I_{a0} is derived as the point of intersection with the resistance straight line R_a . The residual voltage at

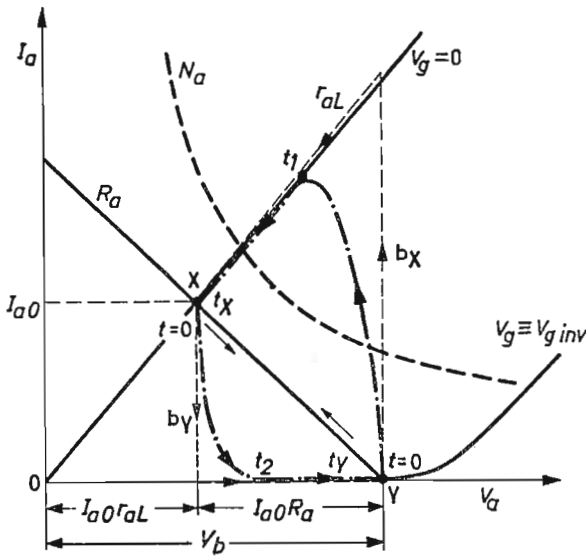


Fig. 3.1 Static and dynamic behaviour of the triode as a switch

the tube amounts to $I_{a0}r_{aL}$, in which r_{aL} corresponds to the limiting characteristic for $V_g = 0$. In the out-position at Y, the anode current is reduced to a negligible fraction of I_{a0} (e.g. under 1%) through the blocking voltage $V_{g inv}$. The feed voltage V_b lies virtually at the anode. The voltage jump at the anode between the opened and closed tube thus amounts to

$$\Delta V_a = I_{a0}R_a \tag{3.1}$$

If the tube is opened or closed by a slow-moving change in grid voltage, the transit behaviour between the in and out positions is determined through the straight line of the resistance R_a . As soon as the rise or fall time of the switch voltage at the grid reaches the dimension of the time constants $R_a C_p$, the transit behaviour at the anode is determined by the parallel circuit of R_a and C_p . This is shown by the fact that the anode voltage can only follow the grid voltage change after a delay. If the opening or closing occurred through a voltage jump at the grid, then, during the switching process, voltage and current would run along the broken lines b_x or b_y . The total anode voltage change would take place with the tube opened or blocked. With finite limits of the grid voltage, transition is brought about within the extremes b_x and R_a or b_y and R_a . On switching on, the control range of the tube is traversed from the instant $t = 0$ up to time t_1 if the blocking voltage

at the grid is exceeded. At point t_1 zero grid voltage is reached. The further course of the anode voltage is determined by the recharging of the harmful parallel capacitance through R_a by the anode current obtained from the limiting characteristic. It is ended at instant t_x if the anode voltage is reduced to the static value $I_{a0}r_{aL}$. The same applies to blocking the tube: At instant t_2 the grid voltage has reached the blocking voltage. The further rise of anode voltage occurs in accordance with the charging up of C_p via R_a through the feed voltage V_b .

As a rule when the tube opens the maximum anode current I_{a0} , as well as the permissible anode leakage capacitance, is momentarily exceeded at the grid; the steeper the flanks of the switch voltage at the grid, the greater the excess. It is therefore necessary to ensure when designing the circuit that the permissible cathode peak current is not exceeded and that the average leakage capacitance does not lie above the permissible anode leakage capacitance — particularly with frequent switching.

To keep the switching times of the tubes, periods t_x or t_y , low, a small blocking voltage, great steepness and a sharply curving $I_a V_g$ characteristic are of considerable advantage. With sufficiently steep flanks to the grid pulse, the sections t_1 and t_2 correspond to only a small fraction of the remaining voltage changes so that for the approximate switching time only the second partial range needs to be taken into account. When the tube opens, the internal resistance r_{aL} then operates in parallel to R_a so that the lagging flank of the anode voltage proceeds with the time constants

$$\tau_{ab} = \frac{R_a r_{aL}}{R_a + r_{aL}} C_p \quad (3.2)$$

or, after the introduction of the anode jump ΔV_a (Equation 3.1):

$$\tau_{ab} = \frac{C_p}{\frac{I_{a0}}{\Delta V_a} + \frac{1}{r_{aL}}} \quad (3.3)$$

In order to maintain a short switch-on time with either a given working resistance or anode voltage jump, the tube must have small capacitances, a small internal resistance r_{aL} and a large anode current.

When the tube is blocked, under the same provisions, we obtain for the time constant of the rising flank of the anode voltage jump

$$\tau_{an} = R_a C_p = \frac{\Delta V_a}{I_{a0}} C_p \quad (3.4)$$

since now the working resistance alone determines the change of load of C_p . The switch-off time of the tube is thus longer than the switch-on time and the greater the internal resistance compared with the working resistance, the larger is this difference (Fig. 3.2). The falling or rising time, t_{fall} or t_{rise} (10 to 90% of the anode voltage jump) is about two or three times the corresponding time constants.

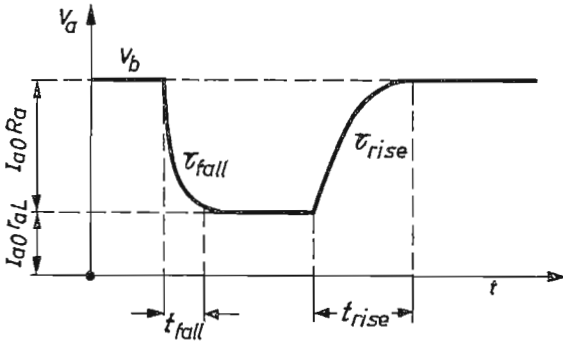


Fig. 3.2 Waveform of the anode voltage at switch-on and-off of a triode (R_a of the same value or greater than r_{aL})

Short switching times thus require a small blocking voltage, a large anode current I_{a0} and small tube capacitances. The blocking voltage is proportional to the anode voltage in the blocked condition, and so to the feed voltage V_b ; so that the proportionality constant approximating to the reciprocal value of the amplification factor μ corresponds to

$$V_{g\text{ inv}} \approx \frac{1}{\mu} V_b \tag{3.5}$$

Tubes with a small value of the reciprocal of the amplification factor and a low anode voltage are therefore convenient. For reasons of safety, so that we are not compelled to work with unnecessarily high blocking voltages, these voltages for the individual tubes should, moreover, vary as little as possible. On the other hand, since with an opened tube the voltage drop produced by the anode current is usually used to block a further tube, the anode current must have the lowest possible tolerances at zero grid voltage. The course of the I_a/V_g characteristic between the blocking voltage and zero grid voltage is only of interest in so far as it helps to determine the minimum switching time of the tube during the control range.

The grid-anode capacitance raises the input capacitance of the tube and reduces its response in multivibrator circuits. It appears at the input of

the tube increased by one factor which corresponds proportionally to the slope of the flanks of the output and input pulses [58].

3.1.2 RELIABILITY AND DURABILITY

Because of the method of operation of the bistable circuits and gates, some tube systems remain without current for long periods under certain working conditions. This method of operation, as we know, is conducive to the intermediate layer formation in the cathode which depends to a great measure on the concentration and nature of the reducing agent in the cathode tube. In this case a layer deficient in barium is formed between the cathode tube and the oxide layer. As far as the current is concerned, the formation of this intermediate layer corresponds to switching a resistance shunted by a capacitance (some 1,000 pF) into the cathode supply line; that is to say, a counter coupling for low frequencies which interferes with the operation of the tube, e.g. in flip-flop circuits. Special cathodes having a weak intermediate layer must therefore be used in tubes for computers to avoid the great influence of this intermediate layer formation on reliability and durability.

The durability refers to the working period during which the tube fulfils certain fixed requirements. These are established for different tubes so that the capacity for work in typical circuits is not impaired within their lifetime. If we plot on a semi-logarithmic scale the percentage of tubes remaining in service against time, the curve shown in Fig. 3.3 is obtained for many types of tube. [26, 27].

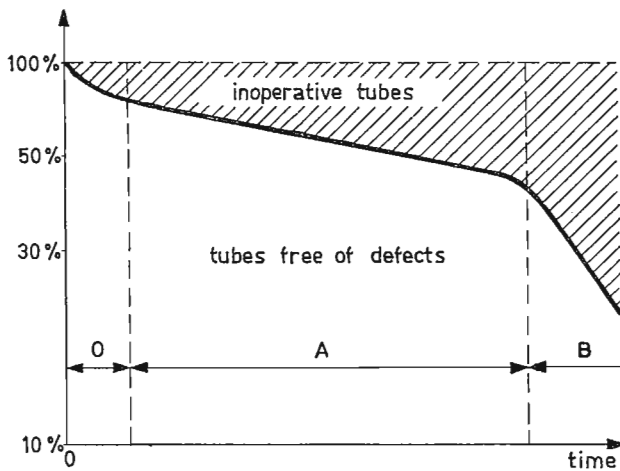


Fig. 3.3 Life curve of a tube type

This is explained as follows: At the beginning, (region O), many tubes show the results of production defects which are not detected during normal factory examination (e.g. break in the electrode supply leads, temporary electrode shorts, etc.). After these tubes are removed, random failures still occur here and there (region A), until finally precise forms of non-random failures predominate (region B), namely those connected with slow-moving physical and chemical processes in the tube (e.g. fall in emission, formation of an intermediate layer, deterioration of the vacuum, contamination or evaporation of the active layer).

Within region A the percentage p of the tubes remaining in operation approximates to

$$p = 100 \times e^{-Pt}$$

The failure of a type of tube is thus indicated by the deficiency index P , the so-called P -factor which is usually given in ‰ per 1,000 working hours. Its reciprocal corresponds to the average durability and is a gauge of the reliability of the type of tube.

At one time the deficiency index was greater in region O, at the beginning of life. The tubes are now pre-fired in the factory and so are more dependable than tubes not so treated.

The lifetime in practice is limited by the bend in the curve in Fig. 3.3 at the transition from region A to region B. Within the practical working life, therefore, we must reckon approximately with a constant tube failure per unit of time corresponding to the P -factor. A replacement of tubes within region A does not reduce the failures. Only at the end of the actual lifetime is it wise to renew the tubes which remain from the beginning.

While the P -factor amounts to about 30‰ per 1,000 hours with normal radio receiving valves, special processes in the construction of long-life tubes have succeeded in reducing the P -factor below 1.5‰. With these long-life tubes, the bend in the curve, the lifetime in practice, lies at more than 10,000 hours. The position of the bend in the curve depends essentially on the working conditions, particularly on the observance of the heater tolerances prescribed in the data. The lifetime of the tube is also determined to a great extent by the actual load of the cathode.

3.1.3 SPECIAL TYPES OF TUBES

Tubes developed according to these standards are the double triodes E90CC, E92CC, E180CC, E182CC, 6463 and E88CC, as well as the heptode E91H with two control grids. These tubes have a comparatively low cathode temperature which is favourable for good insulation between the electrodes.

To avoid intermediate layer formation, the cathode tube is composed of passive nickel with only a very slight silicon content. The most important points of interest in the data of these tubes are the blocking voltages and the anode current for zero control voltage. The tube capacitances are also significant for fast-operating circuits. The double triodes are mainly intended for multivibrator circuits, but they are also suitable for use in gates and similar pulse circuits.

The two miniature types E 90 CC and E 92 CC each have common cathodes and differ only slightly from each other. The E 90 CC is more suitable for circuits which require a small internal resistance, while the E 92 CC has a smaller reciprocal of the amplification factor and a lower grid-anode capacitance.

The noval type E 88 CC with separate cathodes, has a low internal resistance. In addition, the gain and the anode current are greater at zero grid voltage than with types E 90 CC and E 92 CC. Multivibrators using E 88 CC are marked by a high switching speed and great sensitivity.

The double triode E 180 CC, in the noval range, is very similar statically to the E 92 CC, but has a considerably higher permissible peak cathode current (200 mA as against 75 mA).

The noval double triode E 182 CC is marked by a high cathode current (60 mA), a large slope (15 mA/V) and the high peak cathode current of 400 mA. It is therefore suitable for fast-operating circuits and for use when high switch currents are necessary, for example for driving magnetic core stores.

With a maximum cathode current of 31 mA and a pulse peak current of 350 mA, the double triode 6463, also in the noval range, lies between the E 180 CC and the E 182 CC with regard to current load capacity. Its permissible anode load is likewise high (4.4W). It is similar to E 90 CC in other items of data.

Table 3.1. gives a survey of the most important properties of the various double triodes.

The miniature heptode E 91 H (with two control grids) is most suitable for gates and similar coincidence circuits. The two control grids g_1 and g_3 are separated by a screen grid g_2 to avoid reaction of the two switch circuits on one another. A further screen grid and a suppressor grid connected to the cathode lie between the second control grid and the anode.

In contrast to the heptode mixer valves familiar in receiver technique, we aim here at equal control effects for both control grids, as well as low blocking voltages. By suitable grid construction, the tube is already blocked at both grids at -10 V. These low blocking voltages are necessary so that

TABLE 3.1: THE MOST IMPORTANT PROPERTIES OF DOUBLE TRIODES E 88 CC, E 90 CC, E 92 CC, E 180 CC, E 182 CC, E 182 CC AND 6463

	E 88 CC	E 90 CC	E 92 CC	E 180 CC	E 182 CC	6463
μ	33	27	45	50	24	20
S (mA/V)	12.5	6	6	7.5	15	5.2
$I_{k\ max}$ (mA)	20	15	15	20	60	31
$I_{k\ s\ max}$ (mA)	100 ($d = \max. 0.1$; $T = \max. 200\ \mu s$)	75	75	200 ($d = \max. 0.01$; $T = \max. 10\ \mu s$)	400 ($d = \max. 0.02$; $T = \max. 10\ \mu s$)	350 ($d = \max. 0.01$; $T = \max. 10\ \mu s$)
$N_a\ max$ (W)	1.5	2	2	2	4.5 (both systems 8)	4.4 (both systems 7.7)
r_{aL} (k Ω)	2.5	4	7	6	1.5	3.3
$V_{\theta\ inv}$ (V) at $V_a = 150\ V$	6	10	6	7	14	10

μ Amplification factor
 S Slope (mutual conductance)
 $I_{k\ max}$ Maximum cathode current per system
 $I_{k\ s\ max}$ Maximum peak cathode current per system
 d Duty cycle
 T Pulse duration
 N_a Anode leakage capacitance per system
 r_{aL} Internal resistance
 $V_{\theta\ inv}$ Blocking voltage at the grid

we can manage with a small control range at high switching speed. Fig. 3.4 explains the working method of this double control tube. An anode current can only flow if both control voltages are less than the corresponding blocking voltages, i.e. only as long as they are operated in the tetrahedron fixed by the two blocking voltages $V_{g1\text{ inv}}$ and $V_{g3\text{ inv}}$ and the maximum anode current I_{a0} . If the voltage at one control grid is reduced below the blocking voltage, no anode current flows at the other control grid, even at zero voltage. A further speciality of these tubes is the high dissipation of the screen grid, 1 W. When the tube has zero bias potential at grid g_1 but is blocked through grid g_3 , practically the whole of the anode current flows to the screen grid g_2 .

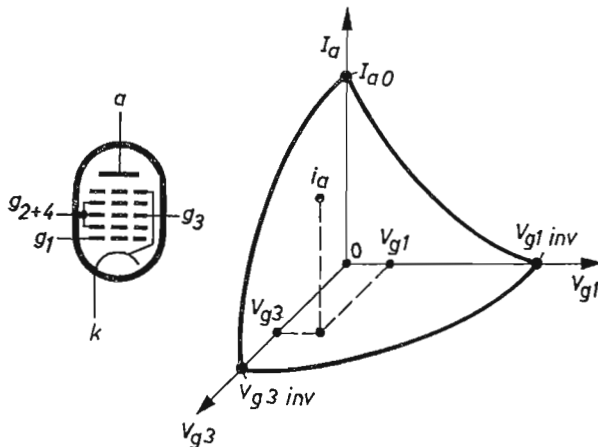


Fig. 3.4 Operation of the heptode E 91 H

The indicator tube DM 160 serves to indicate the condition of rapid flip-flop circuits in which the voltage difference at the anodes is not sufficient to ignite ordinary low voltage neon lamps. Here we have a directly-heated subminiature valve (5.5 mm diam.) which only needs 3 V to control its luminous screen. Because of its low control and filament voltages and small demand for space, it is also well suited for transistor circuits and printed wirings.

3.2. Cold cathode trigger [29]

A trigger tube is a low pressure inert-gas filled tube which has at least three electrodes, i.e. a cold cathode, an anode and a trigger, which has a similar task to the grid of a thyratron.

3.2.1 STATIC PROPERTIES

In a three-electrode trigger tube of this type, six different methods of discharging are usually possible, but only two are important for use in computers, namely discharging between anode and cathode and between trigger and cathode. The working method of a tube so operated is based on the fact that a very small current value between trigger and cathode (transfer current) can trigger off the main discharge between anode and cathode if the anode voltage itself is too low to do this. This transfer current I_{tr} is reduced with increasing anode voltage, as shown in Fig. 3.5. The transfer of the discharging from the priming section to the main section occurs in 10^{-5} to 10^{-4} s. The ignition voltage must operate at the trigger for at least this time.

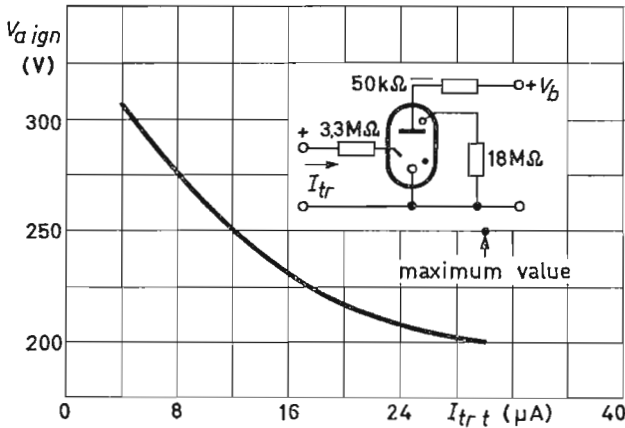


Fig. 3.5 Trigger characteristic of the trigger tube Z 70 U

The two stable conditions employed in the switch circuit technique of computers are the extinguished tube with high anode voltage and zero anode current and the ignited tube with low anode voltage and an anode current of specific value.

Fig. 3.6 shows the ignition characteristic of a trigger tube. To ignite the tube, the point fixed by the anode and trigger voltages must lie outside the ignition characteristic (P_i). To ignite the tube via the trigger, the anode voltage must be under 270 V and above 75 V. In this range, the trigger-ignition voltage is only slightly dependent on the anode voltage.

Variations of the characteristic curve shown in Fig. 3.6 occur with a high resistance ignition circuit if resistances of more than 100 kΩ lie before the

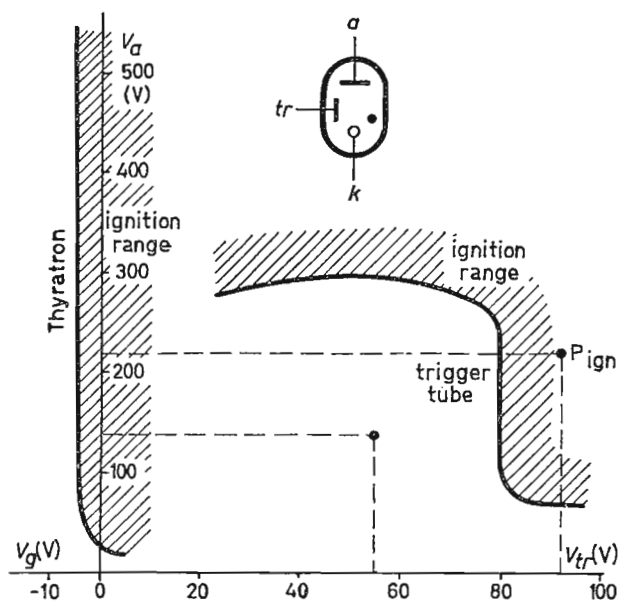


Fig. 3.6 Ignition characteristic of trigger tube 5823. The ignition characteristic of a thyratron (PL 1607) is given for comparison

starter. Then a higher ignition voltage is needed across the resistance in order to reach the necessary transfer current. The ignition voltage at the trigger is increased by rapid successive momentary ignitions of the tube if the mean value of the anode current pulse is less than the minimum current of the normal glow discharge range in the main section.

The characteristic of the main discharge follows the normal pattern of glow discharges (Fig. 3.7). We also see here that the anode ignition voltage depends on the value of the current of the trigger discharge. Within a wide range, the burning voltage is almost independent of the discharge current. The static condition (point *X*) is determined by the resistance R_a in the discharge circuit.

The ignited main discharge can no longer be affected by the trigger. The tube can only be extinguished by a reduction of the anode voltage below the burning voltage.

Since trigger tubes in the extinguished condition are in no way under load, their lifetime is governed by the time of current flow (the time integral of the anode current). As most tubes in computers only carry current temporarily, their durability is considerable. The durability depends chiefly on the peak value of the anode current and also on the number of switchings taking

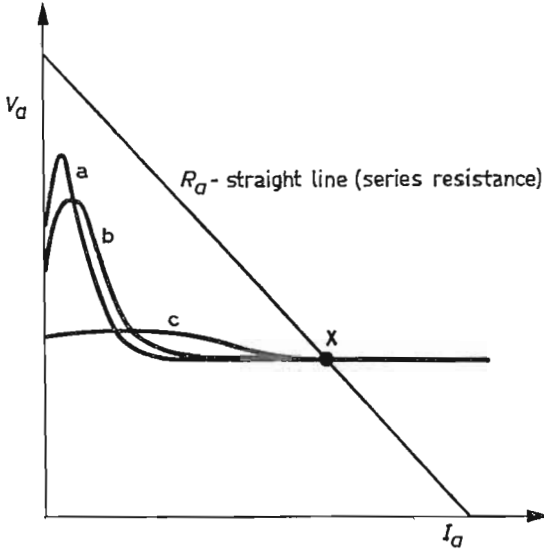


Fig. 3.7 Characteristic of the main discharge of a trigger tube a . . . small, b . . . medium, c . . . large trigger current R_a . . . straight line (series resistance)

place. Further advantages of putting trigger tubes into computers and counters are: Small size, visible indication of their condition, no heating and therefore no energy consumption in the extinguished condition.

3.2.2 DYNAMIC PROPERTIES

As well as the static behaviour, the amount and constancy of the ignition time, composed of the ignition delay and the build-up time, and the recovery time are important factors for including trigger tubes in computers. The recovery time is the least time during which the discharge, from the start of the extinguishing, must be interrupted, so that no re-ignition occurs. [30]. Fig. 3.8 shows the onset of the anode current after the application of an ignition pulse to the trigger which is biased with a voltage V_{tr0} ; the pulse exceeds the ignition voltage V_i by the value ΔV_i . The anode current only begins to flow after a certain time, rising comparatively rapidly (in about 1 to 2 μs). The ignition time is the period from the start of the ignition voltage until the anode current has reached a certain fraction of its end value (e.g. 90%). It depends on the excess voltage ΔV_i and, with ignition by pulses, on the pulse shape and duration. The ignition time is also influenced by the anode voltage, the trigger bias V_{tr0} , the series resistance of the trigger and

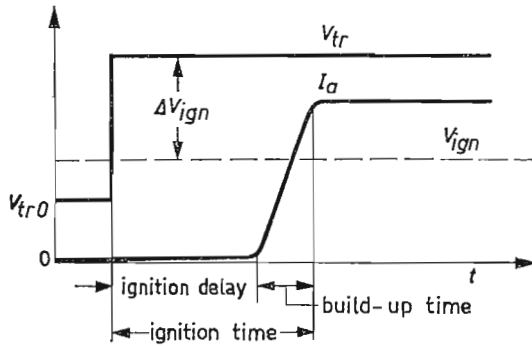


Fig. 3.8 Ignition time of a cold cathode tube

primary cathode (e.g. through a primary discharge). The ignition time with cold cathode tubes amounts to about 20 to 100 μ s.

The extinguishing of trigger tubes takes place as is shown in Fig. 3.9, through a reduction of the anode voltage below the burning voltage V_{arc} to the value $V_{a\ rest}$. Since a finite time is needed to recombine the ions in the discharge space, a precise minimum time must elapse so that the discharge does not continue after the anode voltage is raised to V_{a0} .

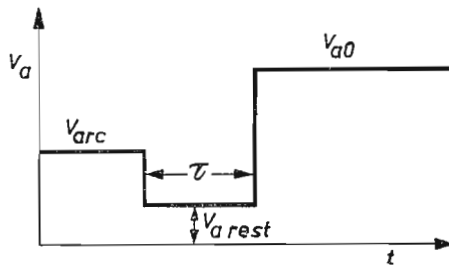


Fig. 3.9 Recovery time of a cold cathode tube

For a certain type of tube this recovery time is dependent on the anode current before extinguishing, the residual voltage $V_{a\ rest}$ and the newly applied voltage V_{a0} , and lies somewhere between 100 μ s and 1 ms. It is greater than the ignition time and determines the maximum switching speed of the tube.

Fig. 3.10 shows the dependence of the recovery time τ on the residual voltage $V_{a\ rest}$ for the trigger tube Z 70 U. τ thus has a minimum if the residual voltage corresponds to a specific fraction of the feed voltage V_{a0} .

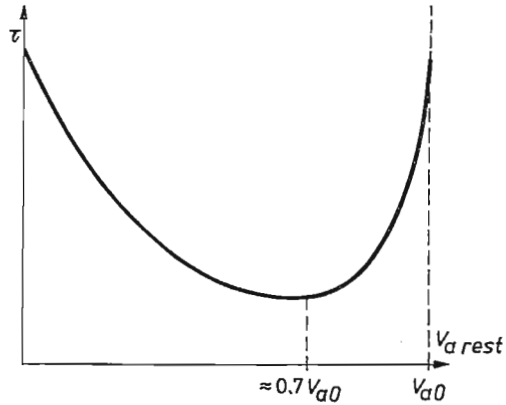


Fig. 3.10
Dependence of the recovery time τ
on the anode voltage $V_{a \text{ rest}}$
(Z 70 U)

3.2.3 THE COLD CATHODE TRIGGER TUBES Z 70 U AND Z 70 W

The Z 70 U is specially designed for use in computers, for example, as a bistable element for switching purposes in counters and stores. It is a four-electrode trigger tube of subminiature type (25 mm long, 10 mm diameter). It contains a pin-shaped priming electrode which is brought very close to the anode and a negative voltage across a large resistance (10 M Ω). By this means a glow is produced during operation, between the priming cathode and the anode which ensures that a certain minimum number of ions is constantly present in the tube; the ignition time is reduced in this way, and to a great extent is freed from the effects of lighting and cosmic radiation. With these tubes, the method of molybdenum spraying and the choice of pure materials have resulted in particularly small leakages of burning and ignition voltages and a high constancy of this value during the working lifetime. At 250 V anode voltage the ignition voltage amounts to 145 ± 6 V; the anode current range lies between 0.5 and 5 mA. The trigger transfer current for ignition is about 20 μ A. The minimum recovery time is 200 μ s when $V_{a0} = 280$ V and $I_a = 4$ mA. The maximum counting frequency lies at about 3 kc/s. The tube can be directly soldered into the circuit and is particularly suitable for inclusion in printed circuits.

In its electrical properties, the Z 70 W corresponds to a great extent to the Z 70 U, but it contains two trigger electrodes. Forward and backward counters can be simply constructed with this type of double trigger tube.

3.3. Semiconductor diodes

Although there are no precise data concerning the durability and reliability of semiconductor diodes, as is the case, for example, with tubes, it can be

said even now that these qualities are higher than with tubes. The chief cause of failures and gradual ageing is the infiltration of dampness or other foreign substances into the crystal surface so that tight encapsulation and correct selection of fillers between crystal and casing are important production problems.

The characteristic properties of a semiconductor diode are the voltage limits in the blocking direction, the limiting of the current in the transmission direction, the magnitude and voltage dependence of the blocking and transmission resistances, as well as the scattering and temperature dependence of the characteristic data or curve. In addition to these static properties, the dynamic behaviour of the diodes is of great importance for pulse operation [31]. Here we must keep a watch on the constancy of the pulse characteristic, on the dependence of the capacitance on the blocking voltage and on the differential internal resistance, as well as on the hysteresis phenomena. For quick switching work, the transition behaviour of the diode in switching over from the current passing to the blocking condition and back is particularly important. The inertia phenomena to be observed here have their origins in a storage of holes and electrons (which keep each other electrically neutral) whose movement in the barrier layer is mainly due to diffusion. The effects of inertia operate inductively in the transition from the blocking to the transmission range; the limit between the ranges with the usual germanium diodes lies at about 0.2 V. At the transition from the transmission to the blocking range, the diode operates capacitively with its storage capacitance, likewise in the blocking condition itself. The blocking capacitance, however, is considerably less than the storage capacitance.

The transition from the transmission to the blocking range usually takes longer and thus decides the transition time (recovery time) of the diode to a great extent. We therefore propose to look into this process more closely.

3.3.1 THE BLOCKING INERTIA [71]

Every current conveyed by the diode produces a certain accumulation of charge carriers (both signs) in the crystal. If the diode is suddenly blocked by a negative voltage, a finite time is needed to develop at the barrier layer the reduction in charge carriers characteristic of the blocking condition. On blocking, therefore, a proportionally larger blocking current will still flow in the first instant. The static value will only arise after a definite time, the transit time of the diode. Fig. 3.11 shows current and voltage during this transition. After switching on the blocking voltage V_{D2} which operates

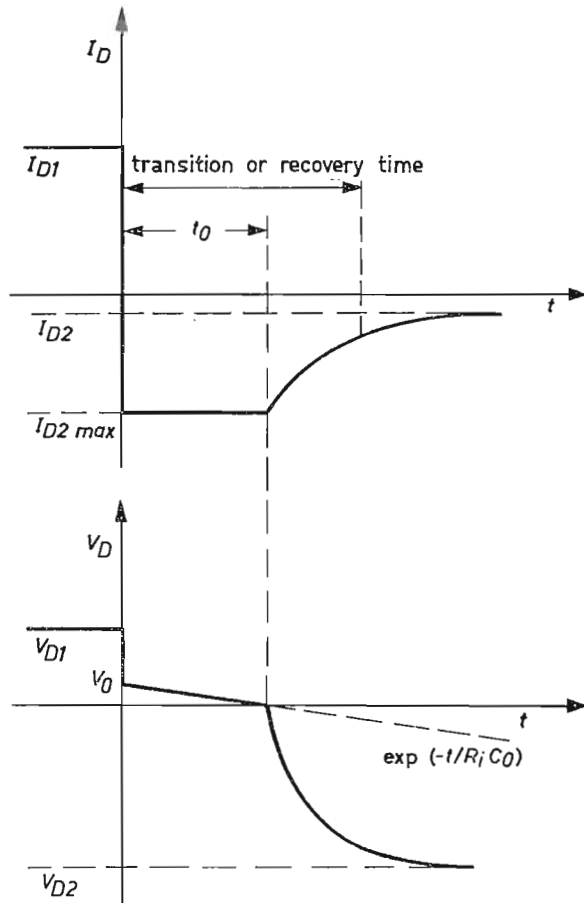


Fig. 3.11
Transit behaviour of a semiconductor diode whose current I_{D1} is switched off by the blocking voltage V_{D2}

via the internal resistance R_i of the voltage source, the voltage over the diode drops practically without inertia to the residual voltage V_0 (≈ 0.2 V) which consists of the diffusion voltage and the momentary potential threshold at the "transition zone". The diode current immediately jumps from I_{D1} to the value

$$I_{D2 \max} \approx \frac{V_{D2}}{R_i}$$

In period t_0 the load Q_0 previously stored by the diode current I_{D1} , is broken down, partly through discharging via R_i , partly through recombination in the diode. During this time the blocking current remains almost constant and the diode voltage drops to zero. The diode behaves approxi-

mately as a capacitance recharged via R_1 from $+V_0$ to $-V_{D2}$. As we know from Fig. 3.11, this storage capacitance has the magnitude.

$$C_0 = \left(1 - \frac{V_{D2}}{V_0}\right) \frac{t_0}{R_i} \quad (3.6)$$

The discharge time t_0 is determined by R_0 , V_{D2} , the storage charge Q_0 (therefore also by I_{D1}) and by the lifetime τ of the charge carrier. Theoretical calculation produces the approximation

$$t_0 = \tau \ln \left(1 - \frac{R_i Q_0}{V_{D2} \tau}\right)$$

The still unknown quantity of charge Q_0 depends chiefly, as is to be expected, on the diode current I_{D1} and also on whether it has been possible to build up the whole charge Q_0 in the previous switching-on time. With a variable diode current I_{D1} the stored charge likewise increases exponentially with time. If the current pulse I_{D1} is of sufficient duration in a diode developed for switching purposes with small spaces between barrier layer and metal, the stationary stored charge is

$$Q_0 \sim \begin{cases} I_{D1} \dots & \text{for small current density} \\ \sqrt{I_{D1}} \dots & \text{for large current density} \end{cases}$$

The storage capacitance C_0 and with it the transit behaviour of the diode are thus determined by the size of the blocking voltage, the internal resistance of the voltage supply, the lifetime of the carriers and the diode current before switch-off. If the pulses are so short that the stationary charge Q_0 cannot yet appear, then C_0 also depends on the pulse duration. As soon as the voltage across the diode has disappeared ($V_D = 0$) and the barrier layer is therefore repolarized, the blocking current gradually drops to its static value I_{D2} , and the diode voltage reaches the external blocking voltage V_{D2} by the simultaneous removal of the residual charge. If we base a time constant τ_s on this approximation of the exponential course of current and voltage, the behaviour of the diode now corresponds to the capacitance

$$C_s \approx \frac{\tau_s}{R_i}$$

This blocking capacitance is considerably smaller than the storage capacitance C_0 . (In Equation 3.6 we have $-V_{D2}/V_0 \gg 1$).

For a quantitative description of the transit behaviour, mostly resulting from the expression of several current values at certain moments after switch-off, it is necessary to give the diode current (which flowed before

switching off the diode), the applied blocking voltage and the internal resistance of the source of the blocking voltage. The transit time defined in this way is in general of the order of microseconds.

The transition from the blocking condition into the transmission range is also connected with inertia phenomena, as mentioned above, since a current only begins to flow when the diffusing defective electrode current reaches the metal electrode and the storage charge is built up (inductive behaviour). The switch-on time, however, is generally less than the switch-off time.

To measure the switch-off time, the diode, carrying a specific transmission current via a square-wave generator with defined internal resistance, is periodically blocked through a certain voltage and the progress of the blocking current is checked by an oscillograph. The switch-on time is measured by sending a constant current of definite value periodically through a diode which is at first blocked with a definite voltage.

3.3.2 LOAD CAPACITANCE

The limiting values for the current and voltage load of a semiconductor diode are determined by the permissible crystal temperature (e.g. 75 °C) and the break-down voltage. The maximum voltage in the blocking direction must lie, for adequate protection, below the break-down voltage. The heating of the diode in the blocking condition gives a second limit to the blocking voltage, depending on the load in the transmission direction and the ambient temperature. Since the residual current increases exponentially with the crystal temperature, (a temperature rise of about 8 °C doubles the residual current), the blocking voltage should only be chosen so high that with the prevailing crystal temperature at the moment of switch-off, the temperature does not rise further.

Provided the transmission and blocking periods are sufficiently above the thermal time constant of the limiting layer (integration time, for example, 50 ms), the crystal temperature in the transmission condition is obtained from the relation

$$\vartheta_{jD} = \vartheta_{amb} + KN_D \quad (3.7)$$

when ϑ_{amb} is the ambient temperature (without additionally disturbed air) and K is the specific heat resistance of the diode. K gives the temperature rise in the diode in °C/mW leakage capacitance (e.g. 0.4 °C/mW). The leakage capacitance N_D is calculated from the transmission current and the voltage drop at the anode. The small temperature dependence of the diode voltage

(it diminishes with rising temperature) can thus be ignored in the first approximation.

The current load of the diode is thus limited by the maximum crystal temperature, according to the relation (3.7). After the diode is switched off, the boundary layer is at temperature ϑ_{iD} . We can estimate the diode residual current and calculate the leakage capacitance N_{inv} in the blocking condition for this temperature and for the adjacent blocking voltage, from the characteristic. We then have

$$N_{inv} < N_D \quad (3.8)$$

so the diode cools down again; it is not overloaded. If N_{inv} were substantially greater than N_D , the diode would heat up further. The residual current would rise still more and the diode would become thermally unstable and would be destroyed. Blocking voltage or transmission current must be reduced. The maximum permissible blocking voltage for a particular transmission load and ambient temperature is thus established through condition (3.8).

If the pulse period is less than the integration time of the diode, the heating of the diode is derived from the average leakage capacitance of one period. An explicit calculation of the load limits is difficult because of the temperature dependence of the blocking current.

3.3.3 POINT-CONTACT AND GOLD-WIRE DIODES

The germanium diode OA 86 is suitable for rapid switching of a not too resistive circuit. Here we have a point-contact diode in all-glass technique whose maximum transmission current amounts to 150 mA (peak value) and whose maximum blocking voltage is 90 V (peak value) at 25 °C. The transmission resistance (with 10 mA) is about 100 Ω . The blocking resistance with voltages from 20 to 50 V (at 55 °C) is greater than 400 k Ω . By switching over from 30 mA transmission current to 35 V blocking voltage with 500 Ω internal resistance, the blocking current drops to 380 μ A after 0.5 μ s and to 36 μ A after 3.5 μ s, while the static value amounts to 10 μ A. The maximum ambient temperature is 60 °C. The resistance for zero bias is about 20 k Ω at 25 °C and shows no alteration after 1,000 working hours. At 60 °C this zero point resistance amounts to 7.5 k Ω . The all-purpose diode OA 95 produced in the miniature range is equally convenient.

The gold-wire diodes are useful for low resistance switching purposes. These are made on a germanium base in which the "anode" consists of a blunt welded gold-plated wire connected to the "cathode" by a special shaping process; there it forms the characteristic barrier layer. The manu-

facturing process, in combination with the hermetically thickened all-glass cover, gives very good stability to the electrical properties. In diodes of this type, the electrical properties in the transition range lie between the point-contact and the junction diodes; that is to say, they have a considerably lower resistance in the transmission direction and a higher resistance in the blocking direction as compared with the usual germanium point-contact diodes. To some extent, the switch-over behaviour is not so favourable as with the point-contact diodes because of the greater surface of the barrier layer.

The individual types are chiefly distinguished by reason of their transmission resistance, their peak blocking voltage and their dynamic behaviour, as is shown in Table 3.2. For special uses we usually have to compromise between these characteristic properties.

Table 3.3 shows the transition behaviour at switch-off. Diode OA7 is particularly suitable for rapid switching.

TABLE 3.2: SURVEY OF THE PROPERTIES OF GOLD-WIRE DIODES

Diode	Transmission resistance with $I_D = 10$ mA $T_{amb} = 25^\circ\text{C}$	Maximum blocking voltage (peak value) with $T_{amb} = 25^\circ\text{C}$	Dynamic Behaviour
OA 5	40 Ω	100 V	moderate
OA 7	42 Ω	25 V	very good
OA 9	32 Ω	25 V	good

TABLE 3.3: COURSE OF BLOCKING CURRENT AT SWITCH-OFF OF GOLD WIRE DIODES OA 5, OA 7 AND OA 9

(The values for type OA 5 are mean values and not binding)

Diode	Transmission voltage I_{D1} (mA)	Blocking voltage $-V_{D2}$ (V)	Max. Blocking current $-I_D$ (μA)		
			after 0.5 μs	after 1.5 μs	after 3.5 μs
OA 5	30	35	2500		60
OA 7	5	5	250		25
OA 9	5	5	450	10	25

3.4 Junction transistors [36, 96]

In contrast to their use in amplifier circuits, junction transistors in the pulse circuits of computers are mainly employed as controlled switches. Other demands are therefore sometimes made on transistors in computers [33]. Compared with other switching work, the use of transistors in computers is marked by the switching capacity which here moves as a rule only in the

dimension of several mW to W. The chief requirements for rapidly operating circuits are a high limiting frequency, small internal base resistance and a small collector capacitance.

The behaviour of a junction transistor for switching purposes is governed by the two static conditions, the blocking condition (out-position) and the transmission condition (in-position) as well as the reciprocal transition between the two conditions. While the reliability depends on the static conditions, the maximum switching frequency is determined by the transition behaviour. For this reason, the transistor generally operates in the emitter circuit which makes a current and voltage amplification possible. Fig. 3.12 shows the basic circuit and the collector characteristic field with the resistance straight line R_L , of a p-n-p transistor loaded with a resistance

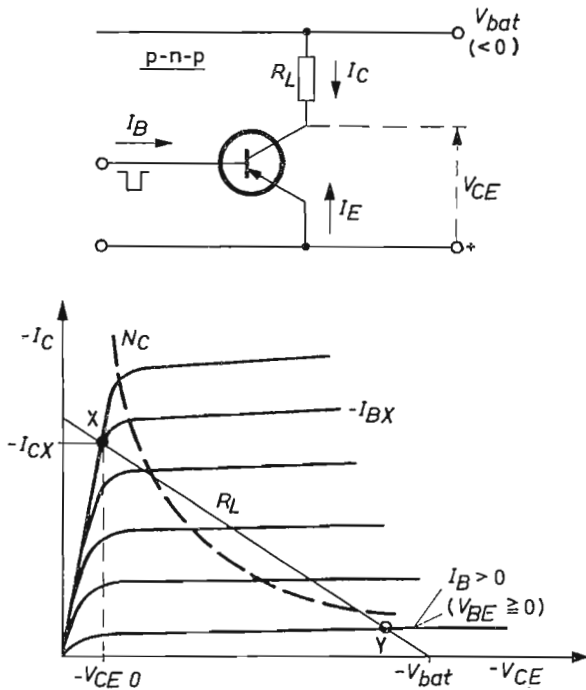


Fig. 3.12 The transistor as switch (in emitter circuit)

3.4.1 STATIC CONDITIONS

We can consider the transistor as consisting of emitter diode, collector diode and internal base resistance. Fig. 3.13 shows an equivalent circuit diagram for the emitter circuit which is sufficient to describe the most important

connections. $R_{bb'}$ indicates the base resistance; the resistances R_e and R_c with the capacitances C_e and C_c serve as equivalents for the emitter and collector diodes. (All these equivalent values are dependent on current or voltage.) In the blocking condition (point Y in Fig. 3.12), the emitter diode is also more or less blocked when the collector diode is blocked, according to the value of the voltage $V_{be'}$ at the emitter diode. With a sufficiently blocked emitter diode, the expression $R_{bb'} \ll R_c || \alpha_e R_e$ holds good for the base resistance (about 50 to 500 Ω), when α_e is the current amplification in the emitter circuit, and in general, $R_L \ll R_c$ for the load resistance. The input resistance of the transistor in the switched off condition then corresponds approximately to the parallel circuit of R_c and $\alpha_e R_e$ with the parallel capacity $C_c + C_e$.

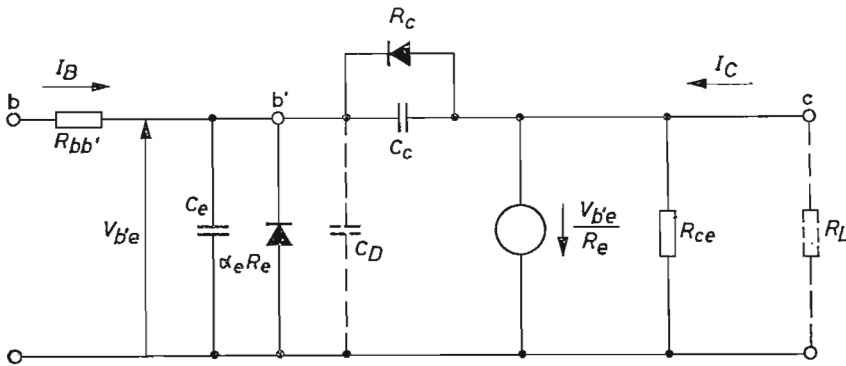


Fig. 3.13 Equivalent circuit diagram of the emitter circuit

The value of the residual current in the out-position can be calculated [41]. Fig. 3.14 shows (not to scale) the qualitative course obtained on the basis of the relation

$$I_B + I_C + I_E = 0$$

In the simplest case, with $I_B = 0$, the collector current I_{CE0} of the emitter circuit flows. (The two first indices denote the electrodes over which the residual current flows.) Through a low positive bias V_{BE} the current is reduced to the collector residual current I_{CB0} of the base circuit (e.g. $10\mu\text{A}$) so that a positive base current flows. The blocking resistance of the collector-emitter section is then in the dimension of several $\text{M}\Omega$. Because of the exponential dependence on temperature of the diode current, all thermal residual currents are also strongly temperature dependent; an increase of

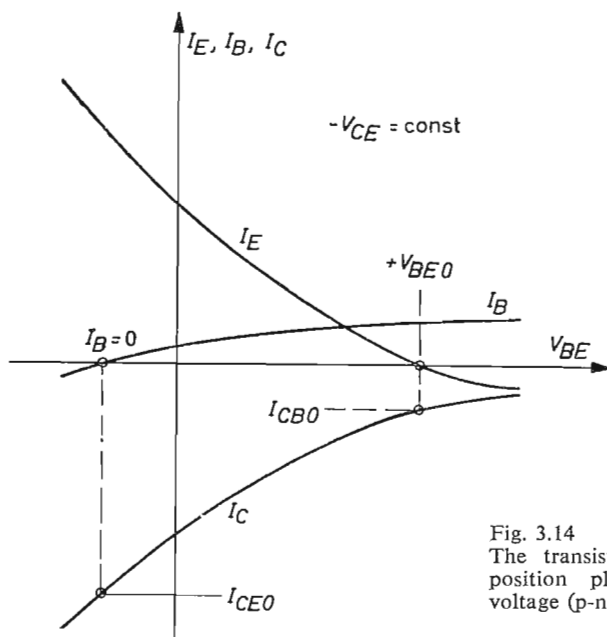


Fig. 3.14
The transistor currents in the out-position plotted against the base voltage (p-n-p type)

about 8°C , for instance, doubles the current I_{CB0} . A reduction of the residual current also raises the thermal stability in the out-position, which will be dealt with later. For the positive base voltage at which the residual current I_{CB0} is reached (neglecting the voltage drop at the base line resistance) we obtain

$$V_{BE0} = V_T \ln \left(\frac{1}{1 - \alpha_b} \right)$$

in which

$$V_T = \frac{T}{11\,600}$$

the temperature voltage in volts (T in $^\circ\text{K}$) and α_b is the short-circuit current amplification of the base circuit. In proximity to the base voltage 0, this is less than the quoted nominal value. For $\alpha_b = 0.9$ and $T = 300^\circ\text{K}$ we find, for example, $V_{BE0} \approx 0.06\text{ V}$. Further increase of the base voltage no longer substantially reduces the residual current; a positive base voltage, however, shortens the switching time, as we shall see later.

The transistor is opened by a sufficiently large base current which controls it as far as the "knee" of the characteristic (point X in Fig. 3.12). This is about the place at which the collector diode passes from the blocking to the

transmission condition. According to whether this point is “evenly” reached or whether the base current is higher than necessary (“overcontrol”), the transition condition during switching is affected on one side and the base and collector leakage capacitances and thus the heating-up of the transistor, on the other.

The voltage drop at the transistor in the in-position, the collector residual voltage $-V_{CE0}$ can be read from the characteristic field. It increases approximately proportionally to the collector current and is very small in other respects. Depending on the value of the collector current it amounts to a fraction of a volt and can therefore usually be ignored in comparison with the feed voltage V_{bat} . The collector current in the open condition of the transistor is thus established approximately through the feed voltage and the load resistance, practically independent of the base current since the characteristics to the left of point X for the different base currents fall closely together:

$$I_{CX} = \frac{V_{bat} - V_{CE0}}{R_L} \approx \frac{V_{bat}}{R_L} \quad (3.9)$$

(with the p-n-p type: I_{CX} , V_{bat} , $V_{CE0} < 0$).

The small residual voltage at the transistor in open condition and the high output resistance in the blocked condition make the transistor very near to an ideal switch.

To attain the opening current I_{BX} , the correct voltage V_{BEX} must be present at the base; V_{BEX} is composed of the voltage drop at the internal base resistance and the drop $V_{be'}$ at the emitter diode:

$$V_{BEX} = I_{BX} R_{bb'} + V_{be'} \quad (3.10)$$

This voltage is also taken from the transistor data so that spreads from specimen to specimen must be taken into consideration.

3.4.2 TRANSIT BEHAVIOUR

The dynamic behaviour of the transistor during on- and off-switching is mainly determined by the inertia of the loads (in the same way as described in Section 3.3.1), by the kind of control, and by its geometry. Basically, the dynamic properties can be obtained from a suitable equivalent circuit diagram of the transistor [21]. However, observing the load carriers in the transistor leads more easily to the objective.

If the transistor is suddenly switched-on by a jump in the base current, the

collector current only rises gradually. In order that a collector current of value I_C can flow, the base layer, as the theory shows, must have the load [72]

$$Q \approx 1.2 \left| \frac{I_C}{2\pi f_{ab}} \right| \quad (3.11)$$

in which f_{fall} is the limiting frequency of the base circuit. The inertia of the leading edge of I_C is now mainly determined by the fact that the base current I_B needs the time

$$t = \left| \frac{Q}{I_B} \right| = \frac{1.2}{2\pi f_{ab}} \times \frac{I_C}{I_B} \quad (3.12)$$

to produce the load Q . To achieve a short switching-on time, we must therefore have the greatest possible base current. In the equivalent circuit diagram this charging time can be allowed for by an additional capacitance between base and emitter through the diffusion capacitance C_D which is substantially larger than the barrier layer capacitance C_e .

With a constant flow into the base (current control), a more exact calculation [41] gives the relation

$$t_{an} = \frac{1}{\alpha_e} \frac{1}{2\pi f_{ab}} \ln \left(\frac{I_{BX}'/I_{BX}}{I_{BX}'/I_{BX} - 0.9} \right) \quad (3.13)$$

for the rise time t_{an} of the leading edge of the collector current. Here I_{BX} is the base current necessary to maintain the collector current I_{CX} (3.9) in the switched-on condition:

$$I_{BX} = \frac{I_{CX}}{\alpha_e} \approx \frac{V_{bat} - V_{CE0}}{\alpha_e R_L} \quad (3.14)$$

in which α_e is the direct current amplification of the transistor in the emitter circuit. (I_{BX} is obtained from the characteristic field in Fig. 3.12). On the other hand, $|I_{BX}'| (> |I_{BX}|)$ is the actual opening current flowing over the base with over-control. We see that the switching-on time rapidly decreases with a growing ratio of I_{BX}'/I_{BX} .

In the case of voltage control (opening the transistor by a voltage jump at the base), the base current changes considerably during switching-on, since the diffusion capacitance must first of all be charged up. As is seen from the equivalent circuit diagram (Fig. 3.13), the base current at the moment of switching-on approximates to

$$I_{BX}(t = 0) \approx \frac{V_{BEX}}{R_{bb'}}$$
(3.15)

in order to drop to I_{BX}' after time t_{rtse} . Here the ratio I_{BX}'/I_{BX} in equation (3.13) is not constant during switching-on. We obtain a rough approximation for t_{rtse} if we substitute for I_{BX}' in Equation (3.13) the mean value from the switching-on peak and static base currents.

Fig. 3.15 shows the course of the current at switching-on with voltage control, i.e. column (a) for not over-controlled operation ($I_{BX}' = I_{BX}$) and

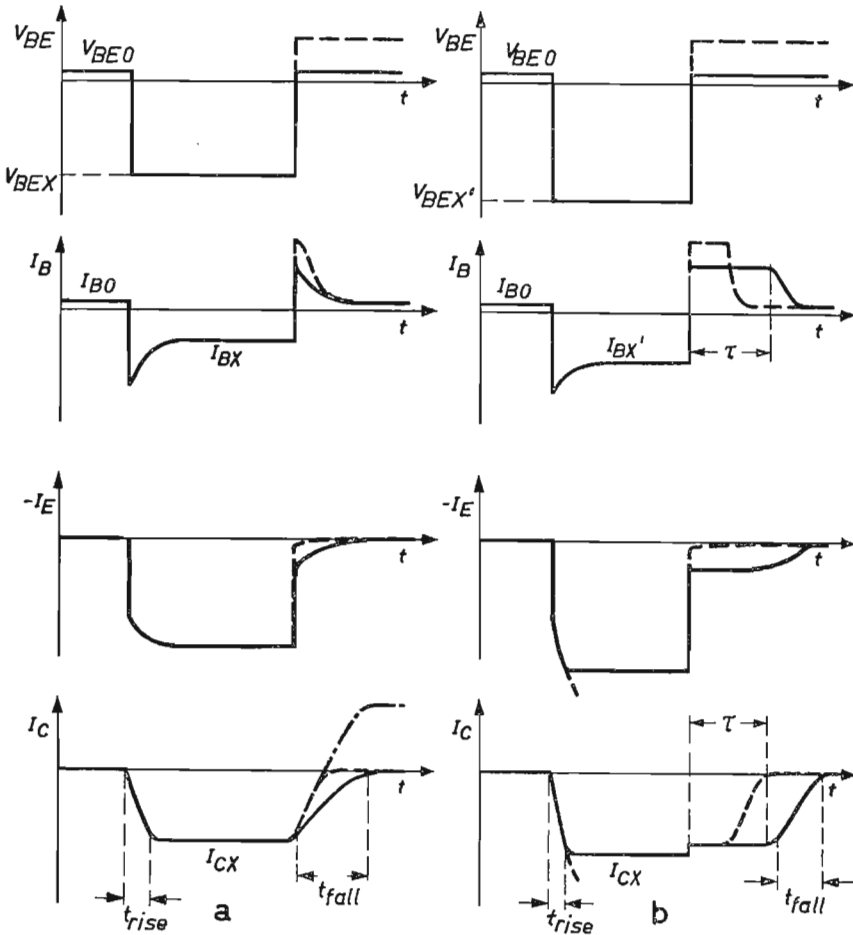


Fig. 3.15 Transistor currents and voltages at switch-over through voltage, in (a) not-over-controlled and (b) over-controlled case.

(b) in the case of over-control ($|I_{BX}'| > I_{BX}$). The transistor is blocked by a low positive base voltage V_{BE0} . If V_{BE} is suddenly made negative, a transmission current flows through the emitter diode, at first mainly towards the base. The main part of the emitter current is only absorbed by the collector after time t_{rise} in which the defective electrons from the emitter are diffused into the emitter zone. In case (a) only the static current of the not over-controlled condition flows into the base. The negative current pulse of the base current at switch-on, seen to the left in Fig. 3.15, is produced in this way, together with the slow increase of the collector current which exactly corresponds to this pulse, since $I_B + I_E + I_C$ must always equal 0.

When the transistor is blocked, other processes take place. If the transistor is not over-controlled, i.e. the collector diode is thus only just in the blocking range, there is a normal exponential discharge of the load. The switch-off time can be shortened here if the base-emitter voltage is positive in the out-condition (shaded curve); then the collector current flows as though it "wanted" to reach a positive control value (dot dash line). In this way we obtain a shorter switching-off time in spite of a more or less equal time constant of the exponential function.

With over-control we now have a case similar to the switching-off of the diode described in Section 3.3.1. The curve for the collector current shown on the right in Fig. 3.15 contains the analogous value τ of the time t_0 indicated in Fig. 3.11.

The storing effect, the base in both cases, is produced here through over-control of the transistor. After the negative pulse at the base is switched off, the emitter diode is again blocked; the surplus defective electrons in the layer, however, keep the collector diode open so that the collector current is maintained during the time τ above. A corresponding reversed base current flows during this period. When the over-control of the transistor is finished, the collector current drops as in case (a). The delay τ , and so the storage time, which can reach considerable values particularly with strongly over-controlled A.F. transistors, is mainly governed by the lifetime of the defective electrons; this depends on the internal recombination and the external discharge via the base current. τ can thus be reduced by increasing the positive blocking voltage at the base since then the defective electrons from the base layer are partly taken over by the emitter (Broken line in Fig. 3.15 b).

The calculation of the storage time shows:

$$\tau = A \ln \left(\frac{-I_{BX}' + I_{BY}}{-I_{BX} + I_{BY}} \right) \quad \begin{array}{l} \text{(with p-n-p-type} \\ I_{BX}', I_{BX} < 0) \end{array} \quad (3.16)$$

in which A is a function of the transistor characteristic value (limiting frequency, current amplification). We see that the storage time is increased with rising $|I_{BX}'|$ and decreased with growing positive blocking current I_{BY} .

The collector current only drops to the residual current within time t_{fall} when the excess loads of the transistor produced by over-control are drained off. For the switching-off time of the lagging edge we find

$$t_{ab} = \frac{1}{\alpha_e 2\pi f_{ab}} \times \ln \left\{ \frac{\left(\frac{I_{BY}}{-I_{BX}} + 1 \right)}{\left(\frac{I_{BY}}{-I_{BX}} + 0.1 \right)} \right\} \quad (3.17)$$

where I_{BY} signifies the base current flowing in the out-position at positive base voltage. I_{BX} is the recombination current in the in-position and therefore not the base current I_{BX}' which is actually flowing. According to Equation (3.17) the collector current drops more quickly the greater the value of the positive bias chosen at the base.

We had an example of voltage control in the two cases shown in Fig. 3.15. As a rule, it provides the shortest switching times and we see that these depend to a great extent on the internal resistance of the control source because of the peaks of the base current during switching. With a large internal resistance of the current source, the base current undergoes no boost, so the switching times increase. We now also see the harmful influence of the internal base resistance since this is in series with the internal resistance of the control source.

We obtain steep pulse flanks and a substantial reduction of the storing effect if we over-control the transistor only during opening, allowing only the necessary recombination current to flow in the opened condition. This can be achieved by series connecting an RC section into the base line as is shown in Fig. 3.16 [34].

The capacitor C is chosen large enough to take the load required for the collector current, thus.

$$C = \left| \frac{Q}{V_i} \right|$$

if V_i is the amplitude of the control pulse. The current flowing in the base then has the value

$$I_B' = C \left| \frac{dV_i}{dt} \right|$$

when dV_i/dt is the flank gain of the input pulse and R_{bb}' can be ignored. The

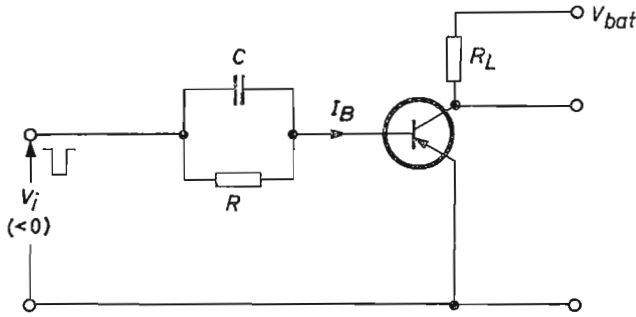


Fig. 3.16 Circuit for avoiding storage effect

resistance R , on the other hand, governs the stationary base current which must correspond to the recombination current (Equation 3.14) to avoid the storage effect. Thus,

$$R = \frac{V_i}{I_{BX}}$$

The harmful parallel capacitance C_p at the collector further flattens the output pulse, particularly its rear flank, as soon as the time constant $C_p R_L$ comes into the dimension of the switching time. C_p therefore limits the load resistance towards high values.

From experience the switching time

$$T = \frac{2}{f_{ab}}$$

can be reached in a transistor with the limiting frequency f_{fall} . Since f_{fall} lies between 300 kc/s and 10 Mc/s with the usual junction transistors, switching times in the μs range can easily be attained. Table 3.4 shows the switch-off times which can be achieved with the transistors OC 71 ($f_{fall} = 500$ kc/s) and OC 46 ($f_{fall} < 3$ Mc/s) at various blocking voltages and opening currents at the base. Switching times of about 1-2 μs can be attained with transistors OC 76 and OC 80.

The measures described above for the reduction of the switching times demand great sensitivity of the circuit in proportion to the spread in the

TABLE 3.4: SWITCH-OFF TIMES OF TRANSISTORS OC 71 AND OC 46 [52]

V_{BEY}	I_{BX}	OC 71	OC 46
0	not over-controlled	6 μs	0.3 μs
> 0	not over-controlled	3 μs	0.15 μs
0	over-controlled	15 μs	0.5 μs
> 0	over-ocntrolled	5 μs	0.2 μs

transistors. By suitable circuit dimensioning, we can thus balance specimen spread against switching speed. Experience shows in this case that transistors with high limiting frequency are preferable even when their spreads work out relatively large.

If we use the transistor in the base circuit, the switching times do not depend to any great amount on the internal resistance of the control source. The storing effect has about the same value as in the emitter circuit with voltage control.

During switch-over the leakage capacitance of the transistor can be higher than the equilibrium value corresponding to the maximum crystal temperature. If the "rest" in this region lasts long enough for the crystal temperature to adjust itself to the transmitted capacitance, the transistor can be overloaded. For example, with frequent switching over, these capacitance peaks contribute substantially to the effective leakage capacitance. In this case, a quick switch-over of the transistor is not only conducive to steep pulse edges and great working speed, but is also advantageous on account of the low heating produced.

3.4.3 THERMAL STABILITY AND CHOICE OF COLLECTOR VOLTAGE

Several points are decisive for the value of the collector feed voltage which, as a rule, corresponds approximately to the output of the switching transistor; these include the thermal stability in the out-position, the switching time and the reliability of the circuit. Similar considerations can be applied for the thermal stability of a switching transistor as with the diode (see Section 3.3.2). Here also, the connection between permissible leakage capacitance and ambient temperature is obtained from Equation (3.7) whereby, strictly speaking, the leakage capacitance is made up of the leakage capacitances of the emitter and collector diodes. In general, however, it is enough to take the collector leakage capacitances into account.

A transistor can be thermally unstable in a circuit if an extensive "feedback" exists between the temperature dependence of the electrical values (particularly collector current and therefore leakage capacitance N_C) and the dependence of the temperature on the heat transmission from the crystal to the surroundings [21]. Any slight disturbance, for example, a small rise in the leakage capacitance, allows the temperature to rise; the residual collector current increases with the temperature and then the leakage capacitance again and so on; that is to say, the transistor can "run away" unchecked at high temperatures. In switching operations, the danger of thermal instability lies mostly in switching off a "hot" transistor from the

feed voltage. With high temperature dN_C/dT_j is large and N_C itself is also proportionally large because of the high voltage. Theory shows [21] that thermal stability can still be guaranteed with reasonable voltages by making use of the maximum crystal temperature only when switching off to a value corresponding to zero emitter current or a base voltage $V_{BE} > 0$. Curves are indicated for maximum collector-emitter voltage for the switching transistors OC 76 and OC 77 which are valid at given ambient temperatures, control voltages and heat resistances. There is also a series of circuits which act as stabilisers [21] but which are generally not practical with capacitive switches because then a loss at the switching capacitance must be allowed for; this could equally well be obtained through a reduction of the operational voltage, restoring the thermal stability.

Further effects of the value of the collector voltage on the switching properties of the transistor are based on the dependence of the expansion of the collector barrier layer on the collector voltage. The higher the collector voltage, the deeper the edge of the collector barrier layer penetrates into the base area. Since this increases the limiting frequency and decreases the diffusion capacitance, a high collector voltage reduces the switching times of the transistor. From the aspect of working reliability, however, a large collector voltage has an unfavourable effect. Apart from thermal instability, there is first of all a danger of reaching the "punch-through voltage," that critical voltage at which the edge of the collector barrier layer extends up to the emitter barrier layer. Further, the relative change of the collector current during its lifetime is greater with high collector voltage than with low. For reliable circuits, therefore, we endeavour to manage with a low collector voltage. It is possible to shorten the switching-off time with a small collector voltage if the collector voltage in the out-position at high feed voltage is limited to a fraction of the feed voltage (e.g. 1/3) through a retaining diode.

3.4.4 SPECIAL TRANSISTORS

Table 3.5 shows the most important properties of some switching transistors. The A.F. transistors OC 71, OC 75, OC 76, OC 77 and OC 80 are most suitable for switching purposes with switch times over 2 μ s. They are marked by their current and voltage load capacity as well as their current amplification. Switching times between 0.2 and 0.5 μ s can be achieved, for instance, with the switching transistors OC 23, OC 46, OC 47 and OC 139. Transistors OC 46 and OC 47 have been developed from the H.F. types OC 45 and OC 44. The n-p-n types OC 139, OC 140 and OC 141 have extensive symmetrical properties (with interchange of emitter and collector).

TABLE 3.5: DATA OF TRANSISTORS FOR SWITCHING PURPOSES

	OC 71/75	OC 76/77	OC 80	OC 46/47	OC 139/140/141	OC 23
f_{ob} (Minimum/value)	350 kc/s	350 kc/s	600 kc/s	3/4.5 Mc/s	3.5/4.5/9 Mc/s	2.5 Mc/s
$-I_{CB0}$ with $-V_{CB}$ (25 °C)	4.5 μ A/4.5 V	4.5 μ A/10V	10 μ A/12 V	3 μ A/5V	3 μ A/5V	30 μ A/10 V
$-V_{CE\ max}$ *)	30 V ($R_{BE} < 500 \Omega$)	32/60 V ($R_{BE} < 1\ k\Omega$)	32 V	20 V	20 V	40 V
$-I_C\ max$ *)	10 mA	125 mA	300 mA	100 mA	200 mA	1 A
	50 mA	250 mA	600 mA	125 mA	250 mA	1 A

*) Permanent values

** *) Pulse loading

As seen from the previous descriptions, we are mainly concerned with information relating to the collector residual current I_{CB0} , the maximum collector voltage $|V_{CE}|$, the maximum collector current $|I_C|$ and the collector residual voltage V_{CE0} , as well as the limiting frequency f_{ab} (in the base circuit for 3 db drop in current amplification) which is closely connected with the minimum switching time. The collector residual current determines the resistance of the switched-off transistor (as well as the thermal stability); the residual voltage determines the resistance of the switched-on transistor; the maximum collector voltage (which depends on the resistance R_{BE} between base and emitter in the circuit) governs the magnitude of the output voltage; and the collector current decides the minimum value of the working resistance in the collector circuit. Table 3.5 gives a summary of the most important data. The types in each column are mainly distinguished by their current amplifications or their limiting frequencies.

3.5 Magnetic materials with square hysteresis loops [38]

The shape of the hysteresis loop of a ferrite depends on its composition and treatment [23]. A naturally rectangular hysteresis loop is obtained, for example, with certain mixtures of the three-substance systems MnO-MgO-Fe₂O₃. A further important group of rectangular ferrites is formed by the system CuO-MnO-Fe₂O₃. Ring cores of such materials can be switched over from the condition of positive remanence into negative remanence or vice versa through current pulses of appropriate direction and specific minimum value in the exciter winding, which induces a voltage in an output winding. By providing a sufficiently rectangular hysteresis loop (normally referred to as a "square loop"), a pulse in the opposite direction, though of only half the strength, or a pulse of any size in the same direction leaves the core practically unaffected. This property makes it possible to use ferrite ring cores of this type with advantage for storage and switching purposes as energy is only needed during switch-over in contrast to similar circuits with tubes or transistors. The great permeability during switch-over and low permeability in the saturation area make square-loop ferrite cores suitable also for magnetic amplifiers wherever there is no need for great saturation induction.

The most important demands made on square-loop ferrites are as follows:

1. A shape of hysteresis loop adapted to the purpose for which it is to be used
2. Small coercive force

3. Short switching times for reversal of magnetisation
4. Low electrical conductivity
5. Temperature- and frequency-constant hysteresis loop
6. Suitable geometric form
7. Mechanical strength

The demands on the hysteresis loop vary somewhat; whether the cores are to be used for switching or storage purposes depends on the different kinds of disturbing pulses to which they are exposed in operation.

Of the three possible preferential directions of the magnetisation vectors in the Weiss ranges, crystal, voltage and shape anisotropy, the crystal anisotropy must be predominant for good rectangularity of the hysteresis loop [23]. This means a low initial permeability [20 to 80] and low shape anisotropy (caused, for example, by pores).

The least possible coercive force (about 0.3 to 1.6 A/cm) is also of great importance in the use of ferrites with rectangular hysteresis loop. On this depends, firstly the number of current windings necessary to reach the maximum induction (about $1,500$ to $2,500 \times 10^{-8}$ Vs/cm²), and secondly the extent of the hysteresis losses which in turn decide the heating of the core and the necessary control capacity. A small coercive force needs a densely sintered material with low crystal energy and little saturation magnetostriction. Since great crystal energy is required on the other hand to prevail over the crystal anisotropy, the demands for good rectangularity and low coercive force are conflicting.

The time needed to reverse the magnetisation of a core limits the operating speed of the circuit. The finite switching time of the ferrites cannot be explained by the inertia phenomena produced by eddy currents, in contrast to metallic ferromagnetics, but appears to be conditioned more by the rotation of the magnetisation vectors in the Weiss areas and their wall displacements [39, 85]. The switching time depends on the amount of coercive force: A small coercive force means a large switching time and vice versa. The comparison of different ferrites as well as the analysis of a material whose rectangularity ratio can be altered under pressure, lead to the rule that the switching time increases with increasing rectangularity. We thus have to compromise in the consideration of switching time, rectangularity and coercive force (and therefore the necessary ampere-turns).

The conductivity of square-loop ferrites must be small enough to avoid the eddy current losses which would be produced with short switching times (0.3 to 12 μ s) and the great induction changes connected with them. Moreover, the Curie temperature should be high (over 300 °C) to avoid strong temperature dependence of the magnetic properties.

With regard to the geometric form in which the rectangular substances are to be used, we generally employ thin-walled rings to obtain the most uniform internal field possible, a prerequisite for achieving good rectangularity of the hysteresis loop. An unhomogeneous field would cause shearing of the magnetisation curve. In order to produce the excitation field strength

$$H_m = \frac{nI_m}{\pi d} \quad (3.18)$$

with the least possible ampere turns (as a rule, only one inserted wire is used), the average diameter d of the rings must also be as small as possible. For storage purposes it amounts to about 1 to 2 mm; for switching, when higher output capacities are needed, we also use greater diameters (e.g. 10 mm).

3.5.1 REVERSAL PROCESS

We now propose to consider the processes at the reversal of a core [68]. The two stable positions of the core correspond to the remanent inductions $-B_r$ and $+B_r$ with the external field $H = 0$. The switch-over occurs through a pulse with the field strength H_m ; its rising time must be small compared with the switching time of the core. The dynamic paths traversed in this case are shown broken in Fig. 3.17. We start from position $-B_r$ and can assume that the induction develops corresponding to section a b. Irrever-

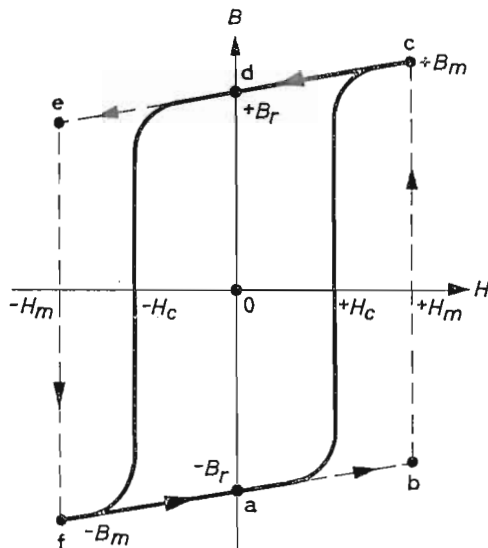


Fig. 3.17 Dynamic path at reversal of magnetisation of a core

sible magnetisation of the core cannot follow the quick field change, so that the induction in the core only rises later within its switching time to $+B_m$. The main part of the change of flow in the core thus drops to the section b c.

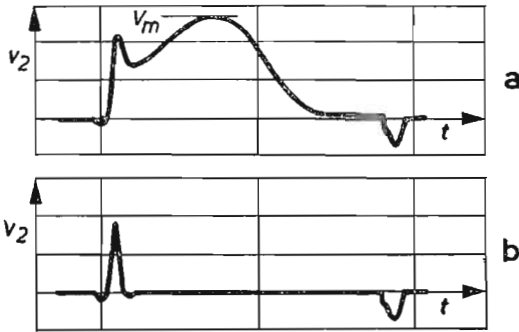


Fig. 3.18 Voltages at the output winding of the core
 a Output voltage at switch-over from $-B_r$ to $+B_r$
 b Interfering voltage with magnetisation in the same direction

Fig. 3.18 shows the pulses arising in this way in the output winding of the core. Its time integral is proportional to the induction change $2B_r$. The first maximum is produced by the rapid reversible change of flow in section a b. The remaining positive portion of the output voltage is derived from the irreversible section b c. The small negative pulse is finally produced via the rear flank of the switch pulse as a result of the reversible change of flow in c d. Physically, the first maximum can be interpreted from the rotation of the magnetisation vectors caused by the reversal of magnetisation, the chief maximum from the wall displacements of the Weiss areas.

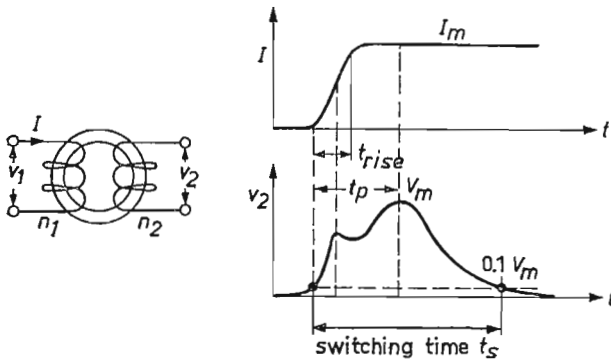


Fig. 3.19 Switch pulse and induced voltage at reversal of magnetisation of a square loop ferrite core

The switching time t_s can be gauged by the period between $0.1 V_m$ at the rise of the output voltage and the drop to $0.1 V_m$, which corresponds to a change of flow in the core of about 90% of the total change. Fig. 3.19 shows the course of the switch and output pulses. It is plain that the duration of the switch pulse must correspond at least to the switching time. With a sufficiently steep switch pulse, the course shown in Fig. 3.20 is produced for the reciprocal value of the switching time, depending on the effective field strength. $1/t_s$ varies approximately linearly with the excitation field H

$$\frac{1}{t_s} = \frac{H - H_0}{S} \quad (3.19)$$

in which $1/S$ is the slope of the straight line and H_0 the distance from zero. S is called the switch coefficient of the material. With modern square-loop ferrites it lies between 0.5 and $1 \mu\text{s A/cm}$.

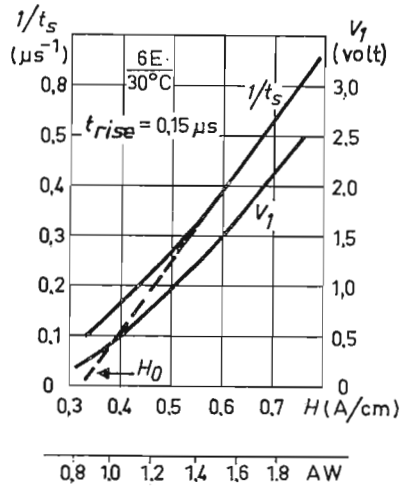


Fig. 3.20 Typical example of the dependence of the reciprocal of the switching time on the switch-over field strength of the core (10 mm core of FXC 6E)

Fig. 3.20 also gives the induced voltage V_1 (per turn) during reversal of the core. H_0 , corresponding to the coercive force of the material, is, however, usually somewhat greater than this. The switching time thus depends on the material and the effective field H_m (core diameter, strength of switch pulses, number of windings). In practical operation, with a finite rising time of the switch pulse, the actual switching time t_s' is also influenced by the steepness of the flanks and the overswing of the pulse.

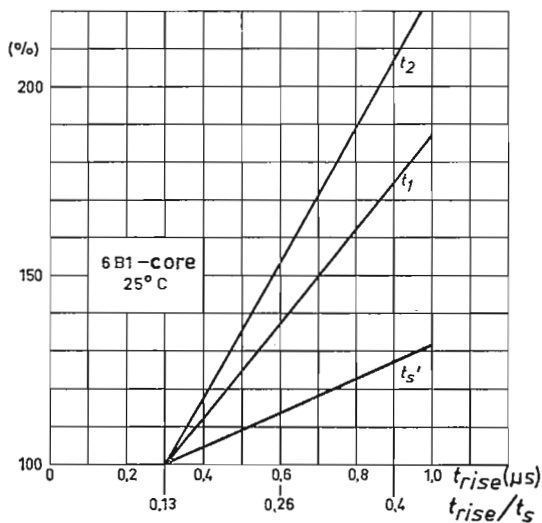


Fig. 3.21
Output voltages and switching times plotted against the rise time of the switch current

Fig. 3.21 shows the dependence of the switching time t_s' on the rising time t_{rise} and on the ratio of the rising time of the switch current to the switching time of the core. Here the percentage change is given as compared with the values given in the data sheets with a rising time of $0.3 \mu s$. Fig. 3.21 also shows the dependence of time t_1 or t_2 for the maxima of the output voltage at the reversal of the core or at half swing.

3.5.2 THE EQUIVALENT CIRCUIT DIAGRAM OF A SQUARE-LOOP FERRITE CORE

The voltage drop at the winding of the core is determined by its inductivity and leakage resistance. While we operate on the level branch of the hysteresis loop, there is usually a reversible inductivity of the core. During reversal, the core works practically as an effective resistance, which is mainly governed by the hysteresis losses during the change of magnetisation.

As long as the core is excited by current strengths which are not sufficient to produce a reversal of magnetisation, it is essentially an inductivity. If we start with half magnetisation reversal current $I_m/2$, we can calculate the permeability occurring here approximately from

$$\mu_r = \frac{B_r - B(I_m/2)}{H(I_m/2)} \approx (1 - \rho) \frac{B_r}{H(I_m/2)}$$

if we introduce the rectangularity ratio

$$\rho = \frac{B\left(\frac{-H_m}{2}\right)}{B_r} \rightarrow 1 \quad (3.20)$$

The reversible inductivity of an unswitched core is then

$$L_r = \frac{\mu_r F \mu}{l_\mu} \quad (3.21)$$

in which $F\mu$ is the cross-section and l_μ the middle path of the field lines. The counter-voltage of a core arising at excitation with $I_m/2$ can now be ascertained from the law of induction by which, owing to the predominance of the reversible magnetisation we can assume that the change of flow follows the current pulse during its rising time t_{an} :

$$|V_r| = L_r \frac{di}{dt} \approx L_r \frac{I_m}{2t_{an}} \quad (3.22)$$

For a 2 mm core of material 6 B 1, for instance, about 15 nH is produced for the reversible inductivity with a rectangularity ratio of 0.9, so that with a pulse rise time of 0.3 μ s, the reversible counter-voltage amounts to about 10 mV. The output voltage induced at reversal is proportional to the change in the ratio $d\Phi/dt$. If we assume in the first approximation that $d\Phi/dt$ is constant during the switching time, we find for the output amplitude

$$V_m \approx n_2 \frac{d\Phi}{dt} = n_2 F \mu \frac{B_r + B_m}{t_s} \approx 2n_2 F \mu \frac{B_m}{t_s}$$

We can now easily estimate the effective input resistance during hysteresis of a core which is not loaded on the secondary. Its primary winding undergoes the constant current influx I_m . Then the energy required for reversing the magnetisation, for example from $-B_r$ to $+B_r$ amounts to

$$\begin{aligned} W_m &= \int_0^{t_s} u_1 I_m dt = n_1 I_m \int_0^{t_s} \frac{d\Phi}{dt} dt = n_1 F \mu I_m \int_{-B_r}^{+B_m} dB = \\ &= n_1 F \mu I_m (B_r + B_m) \approx 2 n_1 F \mu I_m B_r \end{aligned}$$

If we replace the core by an equivalent resistance R_k , the value of this is given by

$$W_m = I_m^2 R_k t_s = \left(\frac{H_m l_\mu}{n_1}\right)^2 R_k t_s$$

in which we have introduced the flow-through $H_m l \mu$. For the equivalent resistance of the core during reversal, related to the square of the number of primary turns, we then obtain

$$r_k = \frac{R_k}{n_1^2} = \frac{2 B_r F \mu}{H_m l \mu t_s} \quad (3.23)$$

Since the product $H_m t_s$ in accordance with Equation (3.19) for $H_m \gg H_0$ alters little with H_m , the equivalent resistance in this range is, in the first approximation, a characteristic value of the core used.

As $d\Phi/dt$ is not constant during switching, this relation produces inaccurate values. The voltage drop at reversal with current I_m corresponds to the secondary output voltage V_1 given (per turn) in the data sheets. We can therefore calculate the equivalent resistance r_k from the relation

$$r_k \approx \frac{V_1}{I_m} \quad (3.24)$$

instead of obtaining it from Equation (3.23).

The energy given off by the core after the conclusion of the driving pulse I_m , because of the change of induction from B_m to B_r is

$$W_r = n_1 F \mu I_m (B_m - B_r) = 2 n_1 F \mu I_m B_m \frac{1 - B_r/B_m}{2}$$

Since the relative remanence B_r/B_m in square-loop ferrite cores lies above 0.9, W_r amounts to less than 5% of the energy put into the cores. W_m is thus leakage energy for more than 95%, i.e. the equivalent circuit diagram of the unloaded core virtually corresponds to an effective resistance.

If the core is loaded on the secondary with a resistance R_2 , the resistance $(n_1/n_2)^2 R_2$ thus appears on the primary in addition to R_k . The current demand of the loaded core thus rises to

$$I_1 = I_m \left(1 + \frac{n_2^2 r_k}{R_2} \right) \quad (3.25)$$

3.5.3 APPLICATION FOR SWITCHING PURPOSES [63, 65, 66, 67, 68]

Ring cores suitable for switching work in logical circuits, shift registers and counters are composed of ferrites or are wound with very thin tapes (0.03 mm) of an appropriate ferromagnetic alloy. As well as one or more input windings and the output winding, the cores usually also carry a pre-magnetising winding which premagnetises the core in the opposite direction, and the switch-back winding (see Fig. 3.22). To reverse the core, the total of all the excitations over a period corresponding at least to the switching time must

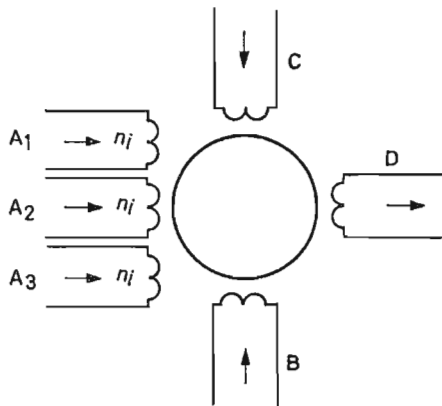


Fig. 3.22

Windings on a switch core
 A_1, A_2, A_3 Input windings
 B Pre magnetisation winding
 C Switch back winding
 D Output winding

produce a field strength equal to or greater than H_m (see Fig. 3.17). The statements in the preceding section are valid with respect to switching time and output voltage.

Switching circuits constructed in this way with magnetic cores can only yield dynamic information, namely the pulses induced during hysteresis. Each working cycle proceeds in two steps: In the first, the result of the logical combination is stored in the core, while the second returns the core to the basic condition through winding C . For magnetic switching circuits we thus need two pulse series displaced by half a period, the first for feeding, the second for the return of the core. Where the logical combination supplies information, pulses of different polarity are induced in both steps in the output winding. According to which of these pulses we use as output pulse, we get in one case almost unretarded information, and in the other information delayed by half a clock period. On the other hand, if the output pulse is produced instead through the defined switch-back pulse, its amplitude and form will be constant to a great extent. In the first case the output pulse (e.g. with the Or-gate) is dependent on the number of input pulses.

If the core is excited with a pulse H_m in the opposite direction, as would be necessary for reversal, the output voltage shown in Fig. 3.18b is produced. It arises from the to-and-fro motion in the sections ab and cd in Fig. 3.17 through the front and rear edges of the switch pulse. This interference voltage is less than the output voltage at switching, and the positive and negative portions are almost equally level because hardly any change of flow takes place. The greater the ratio between output voltage and interference voltage, the greater the suitability of the core for switching purposes.

To keep the interfering pulse as small as possible, the relative remanence must tend as far as possible away from 1:

$$\frac{B_r}{B_m} \rightarrow 1$$

At the moment the attainable values lie between 0.9 and 0.95. Precise demands must likewise be made on the constancy of the input and premagnetisation currents. For example, if the core in Fig. 3.22 operates as And-gate (with three inputs) the winding B must premagnetise the core with $-2H_m$. Then the magnetisation of the core is only reversed if it is excited with $+H_m$ through each of the three inputs. For the maximum permissible input current I_{imax} and the minimum permissible premagnetisation V_{vmin} we must then have:

$$2 n_i I_{i max} - V_{v min} \leq \frac{V_m}{2}$$

so that the core cannot be reversed already by two input pulses. Furthermore, to ensure reversal with three input pulses the condition

$$3 n_i I_{i min} - V_{v max} \geq V_m$$

must be fulfilled for the value of the minimum input current and the maximum premagnetisation.

The permissible fluctuations of the input and premagnetisation currents are established through these relations.

3.5.4 USE IN STORAGE MATRICES

3.5.4.1 Active and disturbing voltage

As well as the regular writing pulse $+I_m$ and reading pulse $-I_m$ (at the coincidence of line and column pulses), cores used in a storage matrix (see Section 2.6.4.2) also receive positive and negative disturbing pulses of the value $I_m/2$ (when a core of the same line or column is written or read), as is shown in Fig. 3.23. These half pulses chiefly produce the following disturbances:

- a) The core is in condition "L" (Fig. 3.24). Then a disturbing pulse $-I_m/2$ causes a drop of the remanance because the magnetisation is partly irreversible so that a small hysteresis loop is passed through. At the same time a disturbing pulse is induced in the output winding of the core corresponding to the associated change of flow. The remanence is reduced

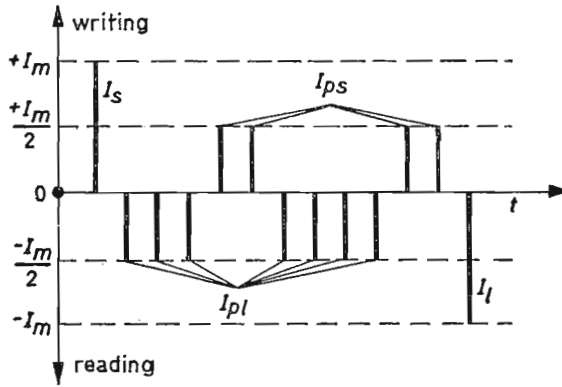


Fig. 3.23 Pulses at a storage element:

- I_s writing pulse
- I_l reading pulse
- I_{ps} . . . interfering pulses in the unselected elements of the chosen line or column during writing
- I_{pl} . . . interfering pulses in the unselected elements of the chosen line or column during reading

in this way through each further pulse $-I_m/2$. With a suitable core material the decline of the remanence is reduced after each disturbing pulse and falls from pulse to pulse to about half the value [75]. The remanence thus rapidly approximates asymptotically to the final value $+B_r^*$ where the magnetisation through the disturbing pulse has virtually become reversible. This remanence $+B_r^*$ corresponds to the disturbed "L".

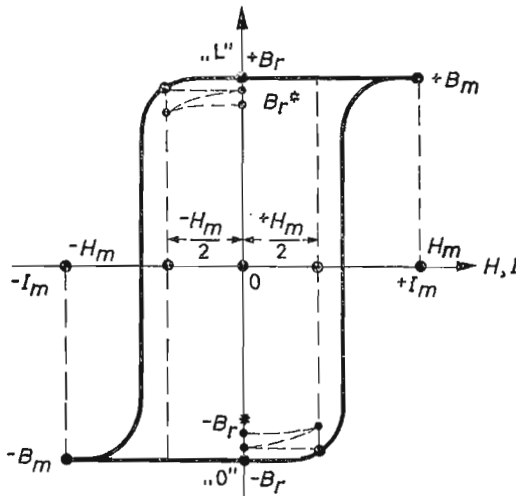


Fig. 3.24 Influence of interfering pulses $\pm I_m/2$

b) The core is in condition "0". Then the negative remanence slips correspondingly upwards with each $+I_m/2$ pulse, and after a certain number of disturbing pulses asymptotically reaches the end value $-B_r^*$ (disturbed "0"). If the core is now read, the output pulse induced in the reading wire no longer has the ideal zero value, but a disturbing pulse is induced corresponding to the induction change $B_r - B_r^*$.

The final values $\pm B_r^*$ are produced at the latest after an eight-fold disturbance with $\pm I_m/2$. The output voltages resulting at the reading of the core, as well as the output voltage for the undisturbed "L" are shown in Fig. 3.25. The time for the maximum and the switching time are thus measured from or to the value $0.1 V_L$. After an adequate number of disturbing pulses there must be enough difference between the reading pulse of the disturbed "L" (case a) and the disturbing pulse at reading the disturbed "0" (case b) for the matrix to work reliably. For this we have the limitation that the remanence B_r is little affected by the half disturbing pulses. This requirement is fulfilled by a hysteresis loop of the greatest possible rectangularity; the rectangularity ratio should, if possible, be 1 (see Equation (3.20)). In practice we reach about 0.9 for this ratio. As a rule, an optimum value can only be obtained with a definite field strength H_m . From experience we achieve the maximum rectangularity ratio when H_m is about 1.3 to 1.5 times the coercive force. For practical purposes it is desirable to have an even course of the rectangularity ratio depending on H_m . Fig. 3.26 shows how the

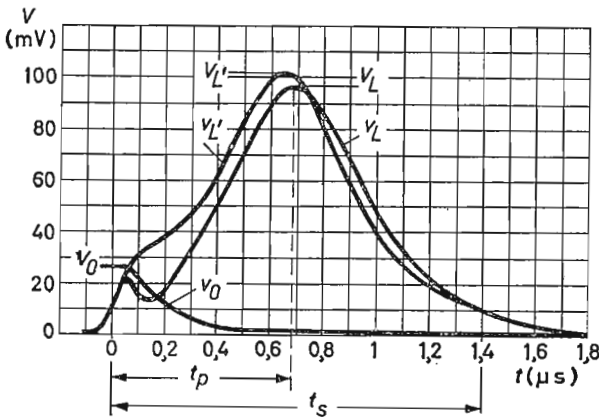


Fig. 3.25 Output voltages at the reading of a core
 V_L' . . . "L" t_p . . . time for V_L
 V_L . . . disturbed "L"
 V_0 . . . disturbed "0" t_s . . . time for V_L

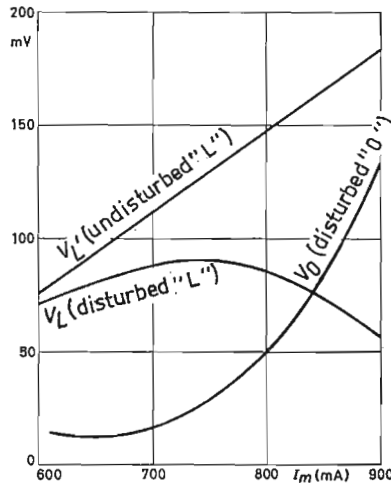


Fig. 3.26 Dependence of the output voltages of a square loop ferrite core on the switch current (40 °C)

output pulse at reading an undisturbed "L", a disturbed "L" and a disturbed "0" depends on the current strength of the switching pulse for Ferroxcube 6 D 3 (the optimum value here lies at about 700 mA).

Since the reversible disturbing voltage is almost proportional to the flank steepness of the driving pulse (see Equation 3.22), the active voltage, on the other hand, depends little on the flank steepness (as long as $t_{rtse} < t_s$); the signal — disturbance interval is greatly dependent on the steepness of the front flank. Fig. 3.27 shows the output voltage V_L at the reading of an "L" and the disturbing voltage V_0 induced by a $I_m/2$ pulse, governed by the rise time t_{rtse} or by the ratio of the rise time of the switching current to the switch time of the core. This gives the percentage change with a rise time of 0.3 μ s compared with the values given in the data sheets. While the active V_L only decreases by a small percentage for a rise time between 0.3 and 1 μ s, the disturbing voltage recedes to about 20%.

Instead of characterising a storage core by the rectangularity ratio of its hysteresis loop, experience shows that it is more convenient to describe its dynamic pulse behaviour in close association with the purpose for which it is used [37], by directly giving the disturbed output signals yielded by the core after engagement by a certain number of half pulses of definite form and value. We usually indicate here the voltage supplied by the core at reading the disturbed "L" (case a) and the disturbing voltage which it yields at the interrogation of "0" disturbed by an equal number of half pulses (case b).

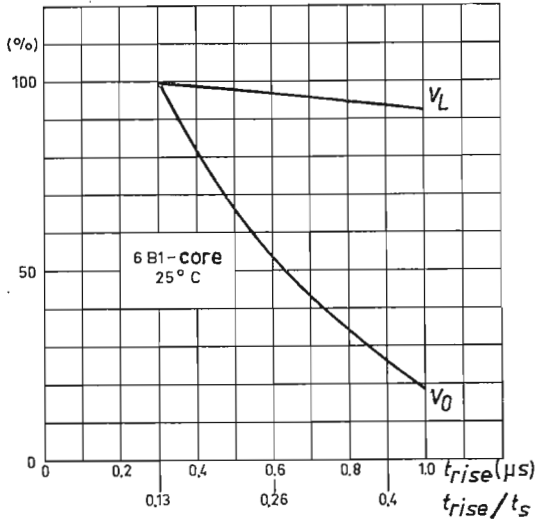


Fig. 3.27 Output voltages plotted against the rise time of the switch current

Between the maximum of the output pulse V_L of the disturbed “L” and the maximum of the disturbing signal produced by the half pulses, there is a time displacement which can be utilised to improve the separation of active and disturbing signals. It can be said in general that on one side, the larger the store, the stricter must be the demands with regard to the disturbance interval, and on the other, the smaller the disturbance interval of the cores in the matrix, the more the outlay increases for the reading circuit.

3.5.4.2 Voltage consumption

The voltage consumption of the individual lines and columns is an important problem, above all with larger core stores. To obtain defined switching conditions for the cores, the switch currents must be drawn from driving stages whose internal resistance lies sufficiently above the resistance of the line or column wires. This is chiefly governed by the inductivity of the unswitched cores as well as by the leakage resistance of the switched cores (as long as the cores are not loaded to any extent). These two conditions occur practically in succession during switching because of the rapid course of the reversible processes with the unswitched cores (see Section 3.5.1). Their dimensional ratio depends with a given type of core on the construction of the store, that is to say, on the number of cores z which must be switched on at the operational maximum of a driving stage, and the total number of cores strung together on one wire.

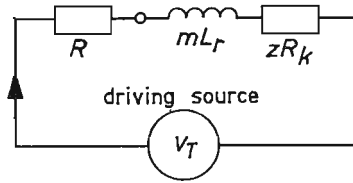


Fig. 3.28 Equivalent diagram of a line or column

Fig. 3.28 shows the equivalent diagram of a line. To evaluate the voltage consumption, we must know the voltage drop at the selected and semi-selected cores. The voltage drop at a core excited with $I_m/2$ was calculated in Section 3.5.2 (see Equation (3.22)). If none of the cores on a wire is switched, the total reversible inductivity of a line or column is

$$L_{rtot} = m L_r$$

If the driving source has the internal resistance R , the time constant L_{rtot}/R must be less than the rise time t_{rise} of the driving pulses to avoid a flattening of their flanks. With low internal resistance (e.g. transistor driving stage), we have to reduce the time constant by connecting in series an additional resistor. So that there is no substantial flattening of the pulse from the driving source, there must be in the line or column circuit a resistor of the value

$$R > \frac{m L_r}{t_{an}} \quad (3.26)$$

The counter voltage of the switched cores runs more slowly, corresponding to the switching time of the cores. It is chiefly determined by the hysteresis loss and the loading of the core and at no charge corresponds to the induced output voltage V_L' (see Section 3.5.2). The counter voltage with z switched cores is thus

$$V_K = z V_L'$$

Since the number of switched cores in storage operation can lie between 0 and z , the irreversible counter voltage of a line or column fluctuates between 0 and V_K . The effective resistance of the line can thus lie between

$$\Delta R = \pm \frac{z}{2} R_k = \pm z \frac{V_L'}{I_m} \quad (3.27)$$

The working method of the store, however, requires approximately constant line or column pulses so that the internal resistance of the driving

source must lie sufficiently above ΔR . We thus have, as the second condition for the series resistance

$$R \gg z \frac{V_L'}{I_m} \quad (3.28)$$

Of the two conditions for R , the one which gives the greater value must be brought in. In coincidence operation this will usually be the value given through the inductive counter voltage (3.26).

Example: 40 matrices with 32×32 cores of type FXC 6 B 1:

$$\begin{array}{r} m = 1280 \\ z = 40 \\ I_m/2 = 225 \text{ mA} \\ t_r = 0.5 \mu\text{s} \end{array}$$

$$R = \left\{ \begin{array}{l} 100 \Omega \text{ from Equation (3.26)} \\ 10 \Omega \text{ from Equation (3.28)} \end{array} \right.$$

With $R = 100 \Omega$ the necessary driving voltage is 22.5 V.

With low resistance driving stages (e.g. transistors) an additional resistance must be connected into the column or line wires, across which a multiple of the counter voltage of the cores is reduced. This means that for transistor driving stages there is a voltage problem as well as a current problem.

3.5.5 RING CORES OF FERROXCUBE 6 FOR STORAGE PURPOSES

Ferroxcube 6 is a ferrite with a rectangular hysteresis loop. This material is available in different varieties which are mostly distinguished by the current amplitude required for writing or reading, and by the switching time. Rings of different sizes are also produced.

The most important properties of the cores, considered chiefly for use in magnetic core stores, are compiled in Table 3.6. The shortest switching times are obtained with cores of the substance 6 F 1, for which, however, an exciter current of 1170 mA is needed. Ring cores of the material 6 E 1 and 6 E 2, on the other hand, only need 350 mA, but they have switching times of about 12 and 8.5 μs respectively. By reducing the diameter to 1.27 mm, the switching time with the 6 D 5 core, for example, recedes to 1.6 μs with approximately the same current.

The values given in Table 3.6 for the output voltages and switching times are based on accurately fixed test conditions for the form, value and number of the pulses applied as well as for the ring temperature. Table 3.7 gives the

TABLE 3.6: THE MOST IMPORTANT PROPERTIES OF DIFFERENT FERROXCUBE 6 RING CORES FOR STORAGE PURPOSES

Typ	6 E 1/6 E 2	6 D 3	6 B 1	6 C 1	6 D 5	6 F 1
External diameter (mm)	3.8	1.95	1.95	1.3	1.27	1.27
Internal diameter (mm)	2.2	1.3	1.3	0.80	0.80	0.80
Height (mm)	1.5	0.58	0.58	0.3	0.38	0.30
Rated value of exciter current (mA)	350 (at 25 °C)	740 (at 40 °C)	450 (at 40 °C)	500 (at 40 °C)	365 (at 40 °C)	1170 (at 40 °C)
Output voltage V_L for 8-times disturbed "L", (mV)	> 37	≥ 87	≥ 68	≥ 36	≥ 40	≥ 110
Output voltage V_0 for 8-times disturbed "0", (mV)	< 6	≤ 29	≤ 21	≤ 12	≤ 13	≤ 31
Switching time t_s (μs)	ca. 12/<8.5	≤ 1.52	≤ 2.25	≤ 1	≤ 1.6	≤ 0.4
t_p (time for V_L) (μs)	ca. 4	0.56-0.71	0.80-1.05	0.36-0.52	0.6-0.8	0.17-0.19

TABLE 3.7: AMPLITUDE OF WRITING, READING AND DISTURBING PULSES FOR DETERMINING V_L , V_0 , t_s and t_p

Typ	6 E 1/6 E 2	6 D 3	6 B 1	6 C 1	6 D 5	6 F 1
Writing amplitude I_s (mA)	350	670	405	450	330	1050
Reading amplitude I_r (mA)	300	670	405	450	330	1050
Disturbing amplitude I_{pi} for the "L", (mA)	213.5 (25 °C)	410 (40 °C)	247 (40 °C)	275 (40 °C)	200 (40 °C)	643 (40 °C)
Disturbing amplitude I_{ps} for the "0", (mA)	183 (45 °C)	410 (40 °C)	247 (40 °C)	275 (40 °C)	200 (40 °C)	643 (40 °C)

values of the reading, writing and disturbing pulses for the test. For reasons of reliability, therefore, the total pulses are selected smaller than the rated current, with the disturbing pulses greater than half the rated current. As Fig. 3.29a shows, the testing pulses can be produced through the aperiodic discharge of a capacitor charged with a definite voltage via a wire fixed through the core, whereby a suitably dimensioned resistance and an additional inductivity are in series. Fig. 3.29b shows the periodic sequence of writing, reading and disturbing pulses when the core is tested. The output voltage V_L' for the undisturbed "L" is produced by the first reading pulse I_l , the voltage V_L for the disturbed "L" by the second reading pulse and finally the output voltage V_0 for the disturbed "O" by the third reading pulse.

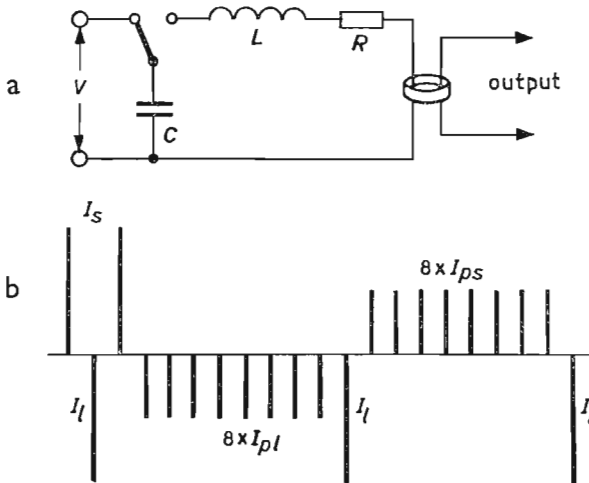


Fig. 3.29 Circuit (a) and pulse series (b) during the testing of a storage core

- I_s writing pulse
- I_l reading pulse
- I_{pl} interfering pulse in reading direction (disturbance of the "L")
- I_{ps} interfering pulse in writing direction (disturbance of the "O")

The output voltages and the switching times depend on the value of the exciter current amplitude I_m and of the disturbing pulse, as well as on the temperature. Figs. 3.30 and 3.31 show this with cores of 6 D 3 and 6 B 1 for the ratios 0.5 and 0.61 of disturbing pulse to complete pulse, and for temperatures of 25 °C and 40 °C. With increasing disturbance ratio, a marked maximum appears for the exciter current of the core, which is moved to lower values at high temperatures. (see Fig. 3.32).

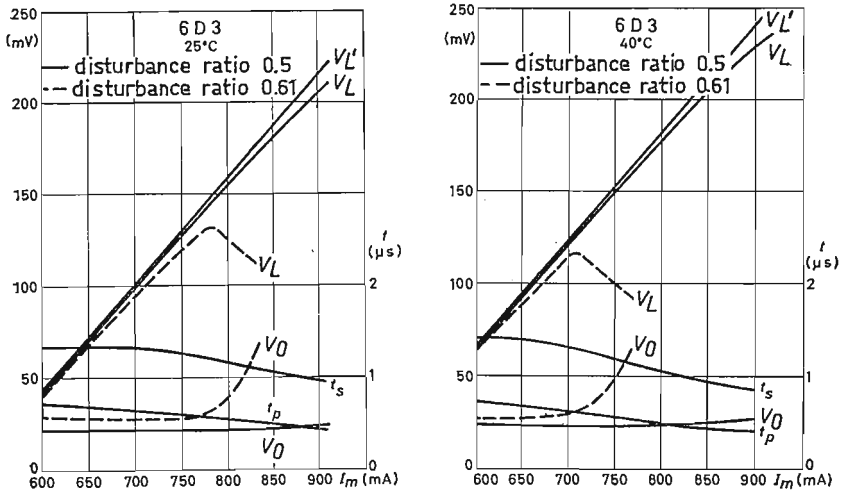


Fig. 3.30 Dependence of the amplitudes of the output voltages and the switching times on the exciter current, the disturbance ratio and the temperature with ring cores of Ferroxcube 6 D 3

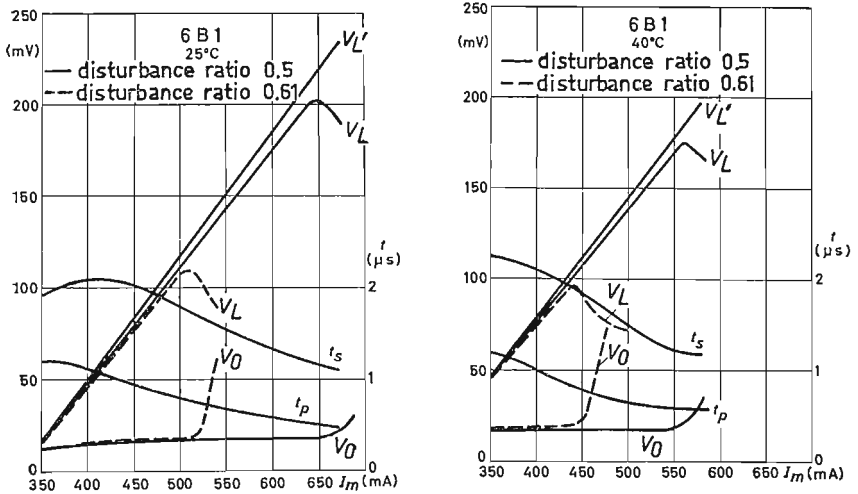


Fig. 3.31 Dependence of the amplitudes of the output voltages and the switching times on the exciter current, the disturbance ratio and the temperature of ring cores of Ferroxcube 6 B 1

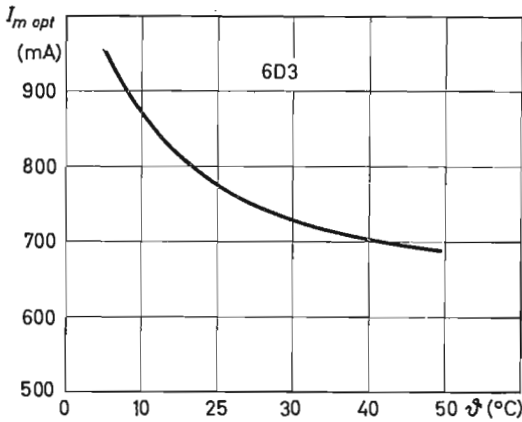


Fig. 3.32 Dependence of the optimum switch current on temperature

3.5.6 MATRIX COMPONENTS

Matrices with, for instance, 32×32 or 64×64 cores are available as magnetic core stores. In a matrix of the type shown in Fig. 3.33, one or two line and column wires, X , Y , are set through horizontally and vertically, as well as the

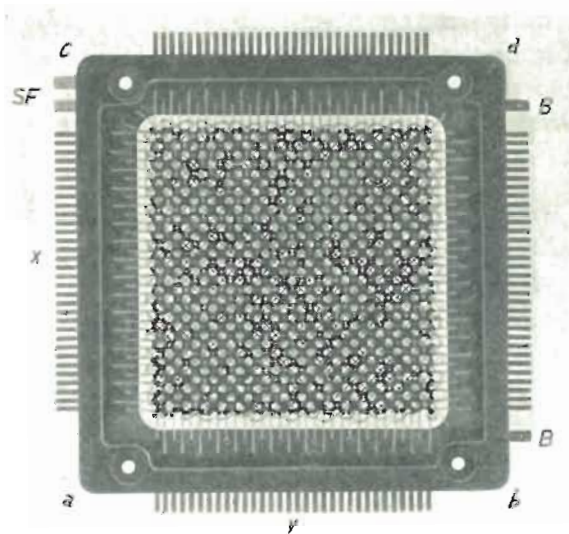


Fig. 3.33 Storage matrix

X line wires
 Y column wires

SF reading wire
 B blocking wire

reading wire, SF and a further line, the blocking wire B , which is also taken through all the cores.

The blocking wire facilitates the half-writing in the matrix of the information read so that it is not lost by the reading (see Section 4.4.4). Here we proceed as follows: During reading each selected core receives a line and column pulse independent of the information to be stored. The blocking wire has the task of eliminating the coincidence in those cores in which an "O" is to be stored. While it remains without current at the writing of an "L", the selected core being thus reversed in magnetisation, it receives a pulse of the value $-I_m/2$ at the writing of an "O", so that the total excitation in the selected core is reduced to $I_m/2$ and the core remains in the zero position. For this purpose the blocking wire must magnetise all the cores in the direction of negative remanence. With a matrix constructed according to Fig. 2.25, this means that it must be led back between the lines before it can pass through the next line. With matrix-construction units, the blocking wire is therefore immediately taken through the next line (see Fig. 3.34). This means that now the direction of flow of the line pulses must change from line to line; this can be arranged if, for example, the even-numbered lines are fed in from the left and the odd-numbered lines from the right. So that the magnetisation of the cores strung on one column wire can be reversed with line pulses of changing direction, the successive cores must each be at an angle of 90° on the line and column wires, as Fig. 3.35 shows. Now the column pulses also must change their course from column to column; only then do we obtain the desired flow through the rings.

When the selected core is read, the reading wire has the task of supplying

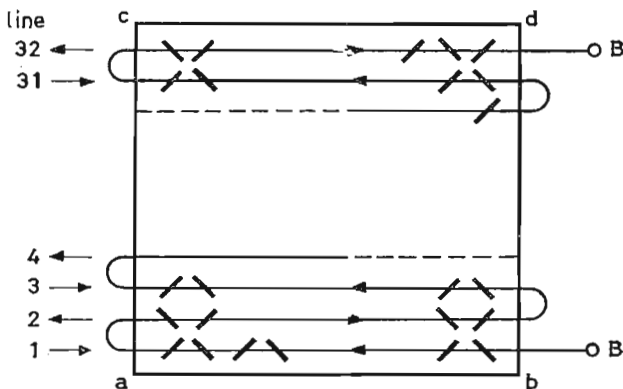


Fig. 3.34 Course of the blocking wire in the matrix

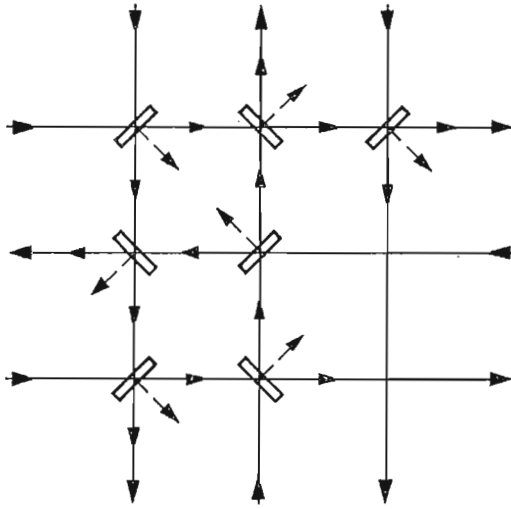


Fig. 3.35 Arrangement of the cores on the column and line wires

an output pulse if this core contains an "L". The wire passes through all the cores and must be led through the matrix in such a way that, if possible, only the output voltage of the selected core can be effective. This requires on one hand a negligible counter inductivity between the reading wire and the line and column wires, and on the other, the prevention of any addition of the disturbing voltages induced when the remaining cores of the selected line and column are read, and produced here through the $I_m/2$ disturbing pulses. This total can be reduced to a minimum if the reading wire is passed diagonally through the matrix, so that successive cores of a line and column run through contrariwise (see Fig. 2.25). This kind of compensation is not complete because the value of the disturbing pulse of a core depends on the core's condition, and thus the resulting disturbing pulse depends on the information stored in the chosen line and column. This residual disturbing signal is a particularly noticeable disadvantage in large storage matrices, and limits their size. We can make use of the so-called Δ -signal of a core to mark this disturbance. This is the difference between the disturbing voltage at reading a semi-selected "L" and that at reading a semi-selected "0".

The counter inductivity to the line and column wires practically disappears if the reading wire is displaced as is illustrated in Fig. 3.36 (shown in two planes for better observation). In this way the cores of each line and column of the reading wire are each passed half-way through in successive perpendicular directions by which the individual counter inductivities are com-

pensated. The halves of the reading wire are connected at corner b; then the reading wire begins and ends at the same place in the matrix.

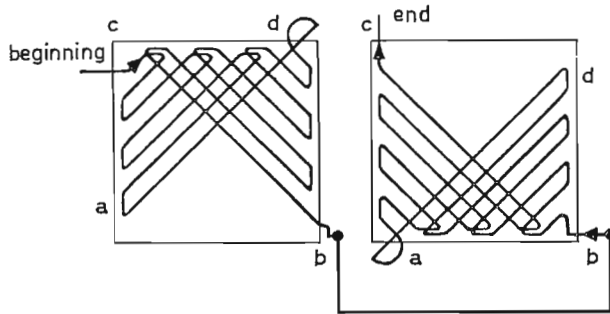


Fig. 3.36 Course of the reading wire in the matrix

In the construction of a store, the single matrix levels are often arranged one behind the other (three-dimensional arrangement of magnetic cores) and the individual line and column wires are also connected in series. On the other hand, the reading and blocking wires remain separate. If we store the bits of a word in successive cores of individual matrices, the whole word can be written or read at one time.

3.5.7 RING CORES OF FERROXCUBE 6 FOR SWITCHING PURPOSES

As already mentioned, ring cores of square loop ferrites are also useful in numerous other circuits as well as in matrix stores, e.g. in logical circuits, counter circuits, registers and as driving stages of core stores. For these uses we have to employ cores with greater diameters for two reasons; First, we must be able to accommodate in the core several windings with different numbers of turns; second, we need greater yields at the output. We thus require more winding space and a larger core volume.

Table 3.8 shows the measurements of a range of switch cores of the material 6 D which can serve, for instance, as driving core for a store con-

TABLE 3.8: DIMENSIONS OF SWITCH CORES OF FERROXCUBE 6 D in mm

External diameter	Internal diameter	Height
5.0 ± 0.25	3.0 ± 0.25	1.02 ± 0.1
8.0 ± 0.25	6.0 ± 0.25	2.03 ± 0.1
13.4 ± 0.45	8.71 ± 0.35	5.59 ± 0.35
26.0 ± 0.85	20.3 ± 0.65	7.21 ± 0.35

sisting of 6 D 3 cores. The hysteresis loop for different controls is shown in Fig. 3.37. The most important data for two different exciter field strengths H_m is included in Table 3.9.

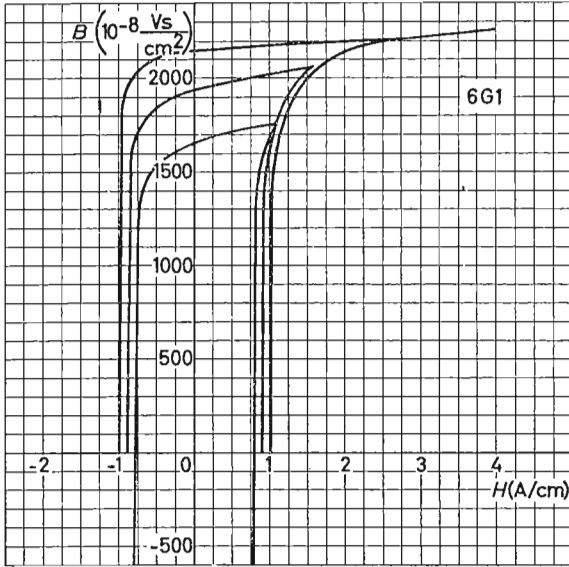


Fig. 3.37 Hysteresis loops for different values of H_m

TABLE 3.9: CHARACTERISTIC DATA OF FERROXUBE 6 D

Maximum field strength (A/cm)	H_m	1.1	2.2
Coercive force (A/cm)	H_c	0.71	0.95
Maximum induction (Vs/cm ²)	B_m	1700 $\times 10^{-8}$	2100 $\times 10^{-8}$
Relative remanence	$\frac{B_r}{B_m}$	> 0.9	> 0.9
Switch time (μs)	t_s	< 2.0	< 1.0

With these values the switch coefficient of the core can be determined from Equation (3.18):

$$S \approx 0.9 \mu\text{s A/cm}$$

The Curie temperature of the material lies above 300 °C. The temperature coefficient of the coercive force amounts to about $-0.2\%/^{\circ}\text{C}$.

Table 3.10 shows the dimensions of two cores of the softer material FXC 6 E; Table 3.11 gives their characteristic data.

TABLE 3.10: SWITCH CORES OF FERROXCUBE 6 E

Type	External diameter (mm)	Internal diameter (mm)	Height (mm)
K5 281 20	9.7 ± 0.2	6.4 ± 0.15	3 ± 0.1
K5 281 25	6 ± 0.15	4 ± 0.1	2.5 ± 0.05

TABLE 3.11: CHARACTERISTIC DATA OF FERROXCUBE 6 E

H_m	0.32	0.44	0.68	A/cm
B_m	1700	2120	2330	$10^{-8} \frac{\text{Vs}}{\text{cm}^2}$
B_r/B_m	0.92	0.94	0.94	
τ_s	10	5	2	μs

Finally, Fig. 3.38 shows the dependence of the maximum induction B_m and the remanence B_r on the excitation in the case of switch core K5 281 20. The greatest possible independence of these values is desirable for many uses of switch cores.

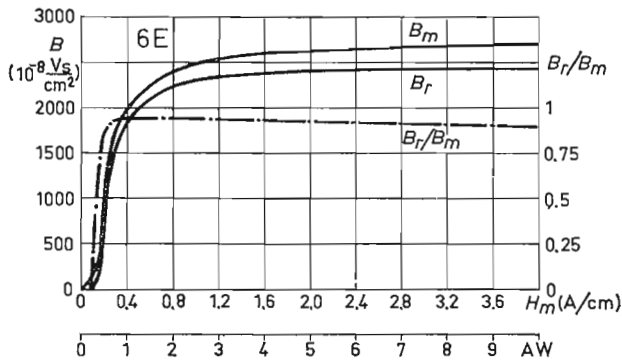


Fig. 3.38 Inductions B_m and B_r plotted against the control for the core K5 281 20

3.6 Magnetic heads for drum stores [25]

The writing and reading of information by means of magnetic heads (in which one head is generally used for both functions), is carried out in the manner described in the working method of the magnetic drum store (2.6.4.1). Fig. 3.39 shows the principle of writing and reading on the magnetisable layer of the drum. The magnetic head consists of a ring-shaped magnetic core which is broken by a small air gap (filled with a non-magnetic substance) and carries a winding. During writing a current supplies a magnetic flow in the winding through core and air gap. The field of the air gap magnetises the drum layer at the place just passed over. During reading the field lines enter the head from the layer whereby they are closed because of the large magnetic resistance of the gap over the core, and a voltage is induced in the coil.

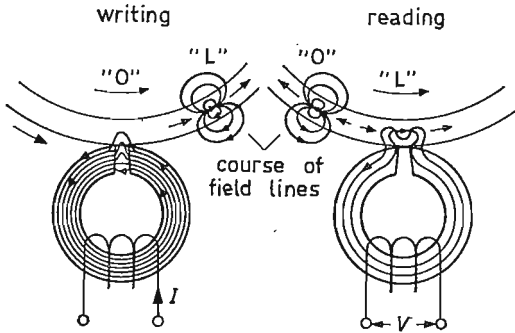


Fig. 3.39 Writing and reading with the drum store

The following properties are characteristic for the suitability of a magnetic material for a writing and reading head: Saturation induction, reversible permeability, specific resistance and mechanical properties.

To make great storage density possible in the drum, layer materials with high coercive force are used so that strong fields are necessary for magnetisation during writing. For that reason, a fairly high saturation induction in the core material of the magnetic head is a prerequisite.

The sensitivity of the magnetic head during reading is obtained through the fraction of the magnetic flow proceeding from the drum which covers the core. This fraction is determined by the ratio between the magnetic resistance of gap and core. A high permeability of the core material is therefore necessary for great sensitivity.

The specific resistance of the core substance should be as high as possible to avoid eddy current losses at high frequencies. In drum stores where the

head is not subjected to wear and tear on account of the distance from the drum, the mechanical properties (hardness, brittleness) are only significant in so far as they have to effect an accurate realisation of the air gap.

The head itself is marked by the shape and size of the air gap, its inductance, hysteresis and eddy current losses and size. The inductance of the head, mostly given by the air gap, determines the energy which must be conveyed to the head during writing. Since the pulse series frequencies lie in the 100 kc/s range, the inductance must not be too high and the magnetic losses must be kept low. On the other hand, the air gap should be small to maintain a comparatively sharply limited stray field to achieve high storage density. In contrast, however, a large air gap is required for great sensitivity during reading.

In comparison with the use of magnetic heads in sound recording or sound reproduction, operation in the drum store is marked by the high frequency range and the spacing of drum and head (e.g. 20 μ). Moreover, no linearity is required here between the current in the coil and the magnetisation in the layer, since only the two directions of magnetisation are to be distinguished. The high frequency range requires small magnetic losses and the spacing between head and magnetic layer stipulates a comparatively large air gap (to give the stray field sufficient depth). We choose it about

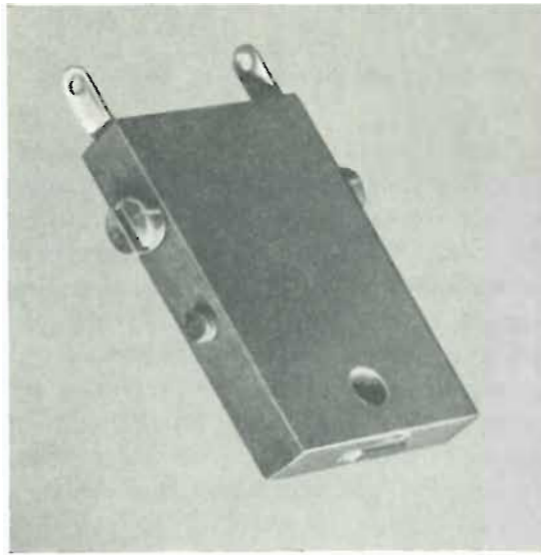


Fig. 3.40 Magnetic head for a magnetic drum store (enlarged about 3 times)

equal to the spacing of the head from the drum. The effective column width on the layer then has about three to five times the value of the gap width of the head and decides the attainable storage density along the drum circumference.

Because of the comparatively large air gap and its consequently large magnetic resistance, adequate reading sensitivity can be obtained with relatively low permeability of the core material. Ferroxcube 3 C 2, with its lower permeability (1100), though higher specific resistance ($80 \Omega \text{ cm}$) as compared with nickel-iron alloys, is thus very suitable for magnetic heads in drum stores. The saturation induction is, however, only about half as great (4650 G) as in nickel-iron. To prevent large eddy current losses, however, the core has to be divided into laminae so that mechanical voltages cannot be avoided. These lower the saturation induction and lead to considerable scattering of the magnetic properties. Fig. 3.40 shows a magnetic head of Ferroxcube for a drum store. The core has a width of 0.8 mm and is embedded in synthetic material. The total thickness amounts to 3 mm. The core, with 50 turns, has an inductance of $45 \mu\text{H}$ and the air gap is 30μ .

EXAMPLES OF CIRCUITS

We have become acquainted in Section 3 with the essential component properties on which their use in computers is based. We shall now deal with the construction of the fundamental circuits described in Section 2. We see in this way that most circuits can be realized with tubes as well as with transistors or ferrite cores and to some extent also with semiconductor diodes. The transistor circuits given here are all constructed with p-n-p transistors. In principle they are also suitable for n-p-n transistors as long as attention is paid to the change of poles of voltages and currents.

4.1 Logical circuits

With these simple and much-used basic circuits, we usually have two different cases, depending on whether their inputs are coupled directly or capacitively. Direct coupling must be used when the input concerned is to be controlled from a static source, for example, from a bistable flip-flop circuit whose rest time in the two conditions can be of any length. Inputs controlled by pulses, on the other hand, can be capacitively coupled, and it is necessary to ensure here that no disturbing potential displacements occur after the coupling capacitor.

Diodes and transistors can be used with advantage for the construction of gates. Since diode gates can only be weakly loaded, a separator stage (resistance-transformer) frequently has to be intermediately connected at their output. The characteristics of transistor circuits are the small residual voltages in comparison to the signal voltages, which makes the coupling of further circuits particularly easy.

4.1.1 REVERSAL CIRCUITS

The reversal circuit serves to change the polarity of pulses and for the interchange of voltage levels. It can be constructed with tubes, transistors and ferrite cores.

4.1.1.1 Reversal circuits with triodes

The circuit shown in Fig. 4.1, for example, transforms the "L" represented by a positive pulse V_L into a negative pulse $-V_L$.

The tube is blocked by the negative grid bias V_g . Output B then lies in the middle of the voltage divider $(R_a + R)/(R_a + R)$. It thus has zero potential. The tube is opened by a positive pulse V_L ; its anode voltage drops and with suitable measuring of resistances R_a and R , the voltage at the output falls to $-V_L$.

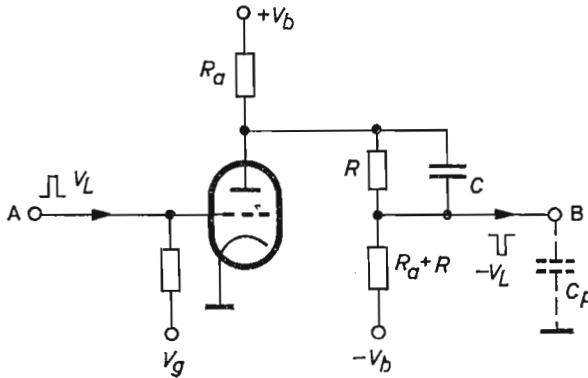


Fig. 4.1 Reversal circuit with a triode

To compensate for the influence of the harmful parallel capacitance C_p (switch capacitance and input capacitance of the succeeding circuit) on the voltage divider, capacitor C is connected in parallel to R . The value of C is derived from the equality of the two time constants RC and $(R_a + R)C_p$. To prevent the relatively high resistance voltage divider from being loaded

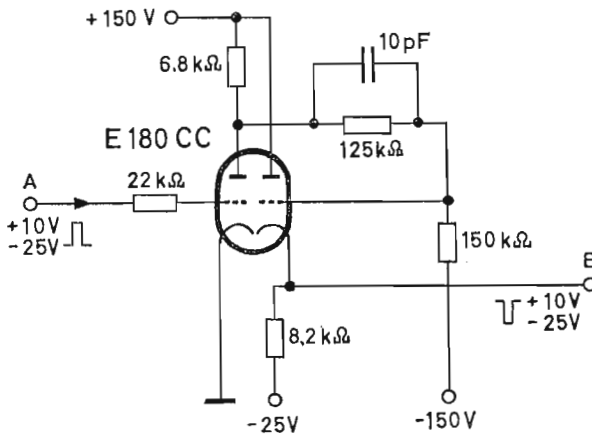


Fig. 4.2 Reversal circuit of the NORC

through the input resistance of the following circuit, a cathode follower operating as resistance transformer must be intermediately connected; the voltage divider mentioned above must therefore be suitable for the control range of the cathode follower.

Fig. 4.2 shows an example for a reversal circuit constructed under these considerations, as employed in the IBM computer NORC. The left-hand system of tube E 180 CC corresponds to the actual reversal circuit according to Fig. 4.1. The right-hand system acts as a cathode follower.

The input pulse goes from -25 V to $+10$ V (the resistance in the grid supply serving as a limit); the output pulse goes from $+10$ V to -25 V.

4.1.1.2 Reversal circuits with transistors

Fig. 4.3 shows a simple reversal circuit with a transistor. The negative pulse representing the "L", for instance, reverses the base from the blocking voltage V_{BEY} to the transmission voltage V_{BEX} , which causes the collector voltage to rise from V_{bat} to the collector residual voltage V_{CEO} , thus almost to zero.

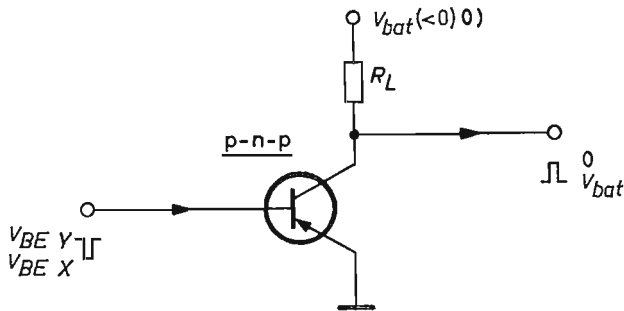


Fig. 4.3 Reversal circuit with a p-n-p transistor

While this circuit corresponds to the tube circuit (Fig. 4.1), Fig. 4.4 shows an arrangement using the symmetrical properties of the transistor which cannot be carried out with tubes [52]. If the positive voltage V_{bat1} is applied at the emitter, the circuit corresponds to Fig. 4.3; we obtain an output pulse of opposite polarity to the input pulse. If we choose a negative emitter voltage V_{bat2} , however, the collector operates as emitter and the emitter as collector. The transistor then works in the collector circuit and we obtain a negative output pulse and thus no reversal. If we place the emitter at the output of a bistable circuit, the circuit then reverses the polarity of the input

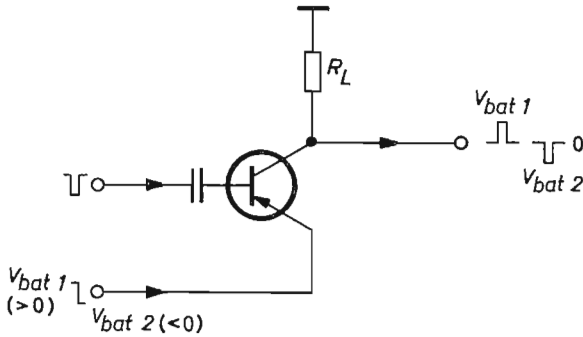


Fig. 4.4 Controlled reversal circuit

pulses at one time and not at another, according to the position of the bistable circuit.

4.1.2 OR-GATE

The Or-gate is a circuit with one output and several inputs; it yields a pulse if a pulse occurs at one or more inputs. As well as logical combination, its task is to unite pulses coming from different sources to one consumer, to prevent reaction between the individual sources.

4.1.2.1 Or-gate with tubes

Fig. 4.5 shows the basic circuit with a double triode. Both systems are blocked by the voltage V_g ; the output has zero voltage. If a positive voltage is applied at input A or B, output C then also gives a positive voltage (of nearly equal value). If the gate is opened at both inputs the voltage is not greatly increased. The cathode current remains approximately constant; the effective output resistance drops to about half, namely to $1/2S$.

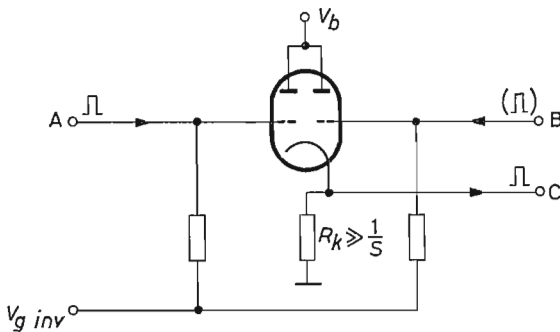


Fig. 4.5 Or-gate with double triode

When we use tubes in the analogous common cathode circuit (Fig. 4.6), there is also a reversal of polarity of the output pulse as compared with the input pulse. A circuit of this type thus represents the connection of an Or-gate with the reversal circuit. To reduce the dependence of the output voltage on the number of opened systems, the working resistance R_a must be chosen sufficiently large compared with the internal resistance r_a of the tube. With a current carrying system, the anode voltage is then already so much reduced that the additional anode current of the other system cannot bring about any substantial voltage change at R_a .

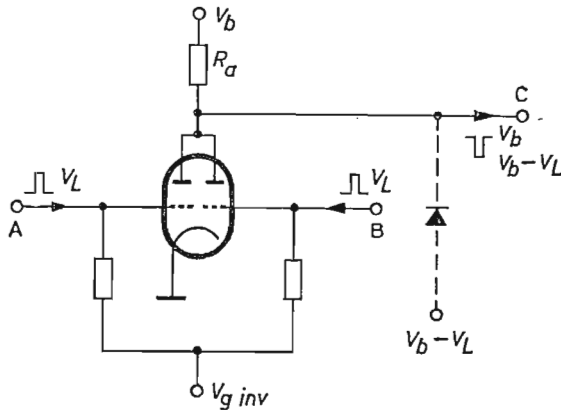


Fig. 4.6 Or-gate and reversal circuit with a double triode

It is a drawback of both circuits that in certain circumstances the rising edge of the output pulse proceeds less steeply than the falling edge because of the different effective load resistances with blocked and opened tubes for the unwanted parallel capacitance (compare Fig. 3.2 and Equations (3.2) and (3.4)).

The working resistance R_a must be small enough to give steep output pulse edges. Then the dependence of the output voltage on the number of connected tube systems can be eliminated through a diode at the output; when the anode voltage drops by V_L through the opening of one system, the diode biased with $V_b - V_L$ prevents a further fall at the opening of a second system.

Fig. 4.7 shows a further circuit constructed with the multi-grid tube E 91 H. Both control grids are at zero bias so that in the absence of input pulses, the output lies below the feed voltage V_b . A negative input pulse, with amplitude corresponding at least to the blocking voltage, at one or both control grids, blocks the tube and causes the anode voltage to rise to

circuit example:
 $V_b = 100 \text{ V}$
 $V_{g2+4} = 75 \text{ V}$
 $R_a = 2 \text{ k}\Omega$
 $V_i = -20 \text{ V}$
 $V_o = +20 \text{ V}$

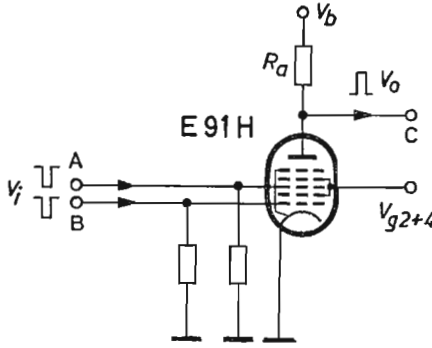


Fig. 4.7 Or-gate (and reversal circuit) with the heptode E 91 H

the feed voltage. The amplitude here is of equal amount for one or both input pulses, independent of the value of the working resistance R_a . R_a can thus be chosen small enough to achieve short rising or falling times for the output pulses. Because of the high internal resistance of the heptode, rising and falling times are also equal here.

4.1.2.2 Or-gate with semiconductor diodes

The construction of the Or-gate is very simple with semi-conductor diodes, so they have a special use for gates with many inputs when we need a diode for each input. Fig. 4.8 shows as an example an Or-gate with three inputs.

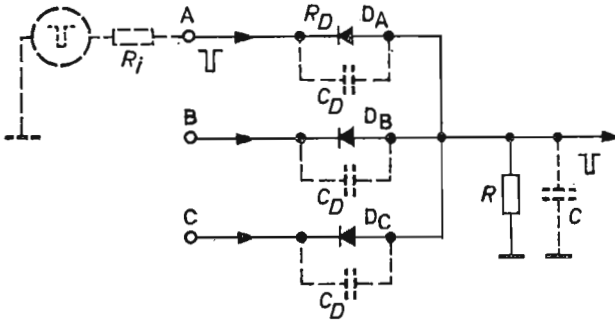


Fig. 4.8 Or-gate with three inputs (direct coupling)

If a negative pulse of value V_i operates at input A, the diode D_A is conducting, and provided its transmission resistance is small compared with the working resistance R , the input pulse appears at the output with full amplitude. This pulse acts as negative bias for the two other diodes so that inputs B

and C are virtually switched off and there is no reaction between the three inputs. If pulses operate simultaneously at two or more inputs, there is practically no change at the output. If the input pulses have different values, the pulse with the greatest amplitude appears at the output. The diodes must be reversed in polarity for positive input pulses.

Through the harmful parallel capacitances, steep pulses appear deformed at the output. If an Or-gate with n inputs is switched in via m inputs ($n > m$), then the capacity of the diodes blocked by the residual $n - m$ operates at the working resistance R as well as the load capacitance C (provided $R_i + R_D \ll R$) so that the equivalent circuit diagram shown in Fig. 4.9a is valid. The front edge is deformed in accordance with the time constant

$$\tau_1 = \frac{1}{m} (R_i + R_D) \times [C + (n - m) C_D]$$

After the cessation of the input pulses, the total parallel capacitance (now $C + nC_D$) must be discharged via R so that here the time constant amounts to

$$\tau_2 = R (C + n C_D)$$

The rear edge will thus be considerably flatter than the front edge (Fig. 4.9).

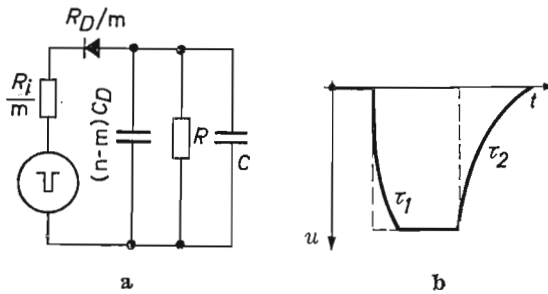


Fig. 4.9 Equivalent diagram of an Or-gate with n inputs, of which m receive pulses (a), and the pulse distortion (b)

If the coupling of the gate should occur capacitively, the relative level of the input pulses must be kept at zero through additional retaining diodes as is shown in Fig. 4.10. The function of the circuit which is also suitable for negative pulses, corresponds in all respects to the circuit according to Fig. 4.8, so that the diodes d , as already mentioned, ensure that the voltages behind the coupling capacitors cannot become strongly positive.

The value of the working resistance R must be so chosen that on one side the time constant is not too large, and on the other that

$$R \gg R_i + R_D \quad (4.1)$$

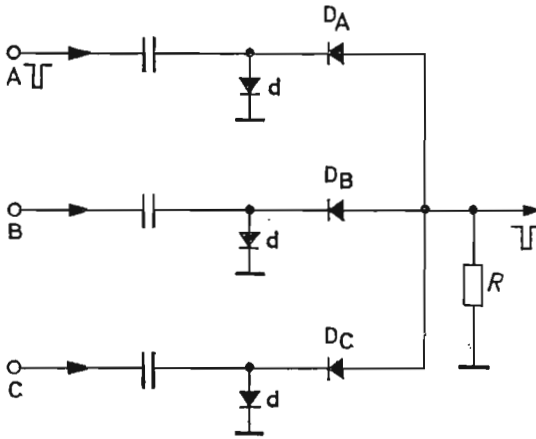


Fig. 4.10 Or-gate capacitively coupled

The permissible blocking voltage of the diodes used must correspond at least to the pulse amplitude V_i . The necessary current load capacity is obtained from V_i/R . Finally, we must pay attention to the recovery time of the diode (see Section 3.3.1) in rapid-operating circuits.

4.1.2.3 Or-gate with transistors

Fig. 4.11 shows an Or-gate with three directly coupled inputs. In the rest

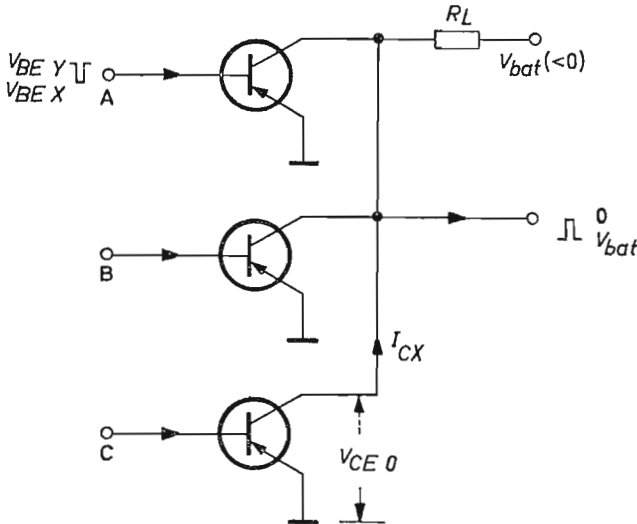


Fig. 4.11 Direct coupled Or-gate (with directional reversal)

condition the blocking voltages V_{BEY} operate at all the inputs; the output is then practically at the feed voltage V_{bat} . A negative pulse at one input opens its transistor; the output voltage rises to zero. The emitter circuit produces a reversal of the pulse polarity. If the gate is opened by several inputs simultaneously, there is virtually no change at the output as long as the load resistance R_L is large enough compared with V_{CE0}/I_{CX} . The number of inputs of this kind of Or-gate is restricted by the collector current in the blocked condition. If the sum of the residual currents approaches the dimension of the transmission current I_{CX} of a transistor, the output voltage jump becomes too small. This is also connected with a displacement of the relative potential.

4.1.3 AND-GATE

The And-gate likewise has two or more inputs and one output; it yields information, however, only when pulses operate at the same time at all the inputs. If the input pulses are of different duration, an output pulse is then only obtained in the overlap period. Apart from binary combinations, And-gates are frequently used as electronic switches (compare Section 2.4.1).

4.1.3.1 And-gate with tubes

The And-gate circuit can be derived simply from the Or-gate by interchanging the resting and working conditions. The circuit is so adjusted that the complete anode current is only suppressed by blocking all the systems. From Fig. 4.5, for example, we obtain the circuit shown in Fig. 4.12. Both systems are opened in the rest condition; the output voltage is high at the cathode resistance R_k . In spite of the blocking of one system, this rest voltage

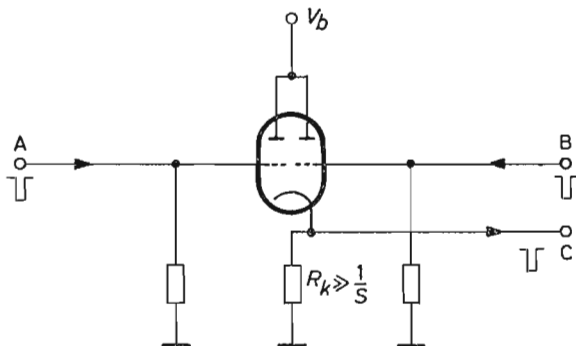


Fig. 4.12 And-gate with a double triode

in C is hardly altered by a single negative pulse. The effective output resistance is raised from $1/2S$ to about $1/S$ in complete conformity with the circuit in Fig. 4.5. The output voltage only drops to zero if both systems are blocked by a sufficiently large negative pulse.

Fig. 4.13 shows the And-circuit equivalent to the Or-gate according to Fig. 4.6. Both systems are opened in the rest condition, and because of the intermediately-connected diode, the voltage at the output can then only rise by the amount V_L if the anode voltage is raised by $2 V_L$. Then the circuit only gives an output pulse when the gate is blocked at both inputs, as the voltage rises from $V_b - V_L$ to V_b .

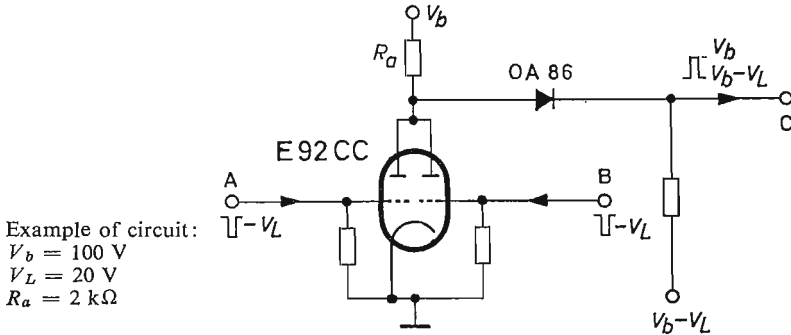


Fig. 4.13 And-gate (and reversal circuit)

The circuit of an And-gate constructed with the heptode E 91 H is shown in Fig. 4.14. The tube is blocked in the rest condition at both grids through

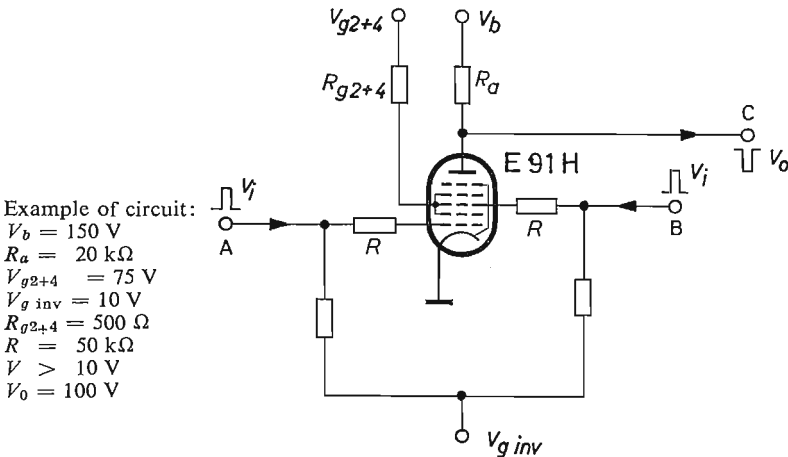


Fig. 4.14 And-gate with the heptode E 91 H

the blocking voltage $V_{g \text{ inv}}$. Then a (negative) output pulse is obtained only if positive pulses ($> V_{g \text{ inv}}$) operate at both inputs.

4.1.3.2 And-gate with semiconductor diodes

As with the tube circuits, we also obtain the And-gate (Fig. 4.15) from the Or-gate by exchange of rest and working conditions. In the rest condition the diodes are conducting because of the positive bias V_R so that the output is kept approximately at zero voltage provided that

$$R_i + R_D \ll R \quad (4.2)$$

If positive voltages or pulses of amplitude $V_i > V_R$ now operate at all the inputs, a positive pulse of the value V_R appears at the output of the

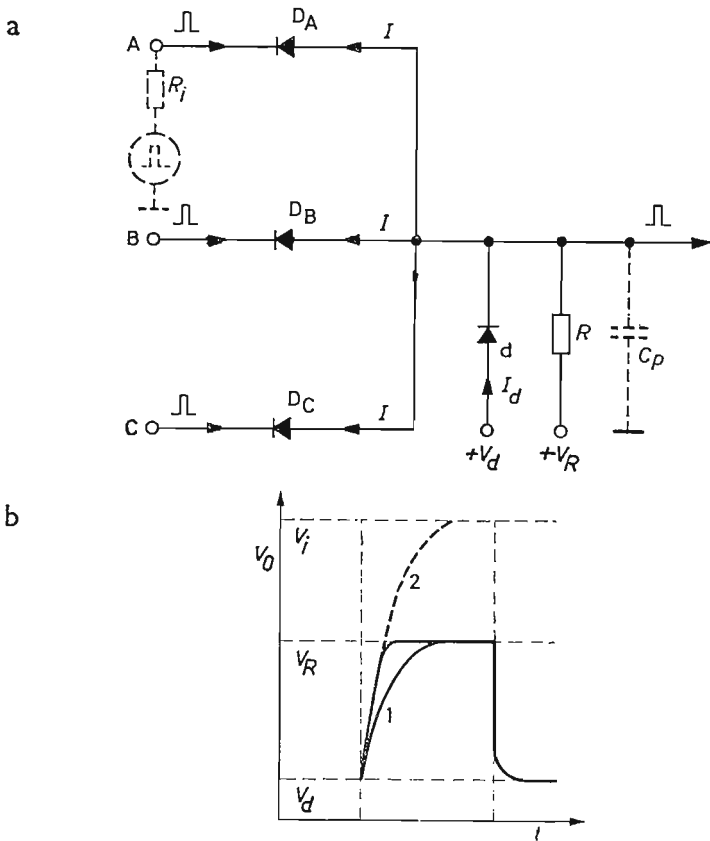


Fig 4.15 Direct coupled And-gate, a circuit, b output voltage

gate since now all the diodes are blocked. If, however, the input voltage is absent at one input, e.g. at B, the output is kept at zero voltage through the diode D_B . The current through this diode (in the open circuit of the gate) then amounts to

$$I_m \approx \frac{V_R}{R}$$

If there are pulses at all the inputs whose amplitudes are all or partly less than V_R , the output pulse then corresponds to the smallest input pulse because the diode concerned keeps the output at this voltage.

Because of the finite value of the internal resistance R_i of the sources, the output will have a reduced positive voltage of the value

$$V_R \frac{R_i + R_D}{m} \left/ \left(\frac{R_i + R_D}{m} + R \right) \right. \quad (4.3)$$

even when coincidence of the input voltages is lacking and m is the number of inputs without pulses. In the case of no coincidence, there will be a more or less large interfering pulse at the output, depending on the number of pulses at the input. This defect can be lessened by the additional diode d which, with no coincidence, keeps the output voltage at V_a practically independent of the number of input pulses. This positive bias must be chosen large enough to remain above the interfering voltage, according to (4.3), even in the most unfavourable conditions, namely when coincidence is lacking at only one input ($m = 1$):

$$V_a > V_R \frac{R_i + R_D}{R + R_i + R_D}$$

The output voltage of the gate is then

$$V_o = V_R - V_a$$

Because of the finite resistance of diode d , the output voltage of the blocked gate is not entirely independent of the number of input pulses, so the smallest possible resistance must be aimed at for diode d .

The course of the output pulse is shown in Fig. 4.15b: At coincidence the recharging of the undesirable parallel capacitance C_p (load capacitance at the output and sum of the diode blocking capacitances) must take place via the working resistance R , i.e. with the time constant

$$\tau_1 = R C_p \quad (4.4)$$

(curve 1). The falling edge, on the contrary, will be considerably steeper since C_p is now also discharged via the internal resistances of the input sources. A shortening of the rise time can be achieved by raising the input amplitude V_i above V_R , since then the exponential function is prematurely discontinued (curve 2).

A capacitively-coupled And-gate is shown in Fig. 4.16. Here the diodes are negatively-biased via the leakage resistances r . In the case of no-coincidence, diode d then keeps the output voltage practically at zero if the condition

$$\left| \frac{V_r}{r} \right| > \left| \frac{V_R}{R} \right|$$

is fulfilled. A drop in the input pulses to a negative value beyond the coupling capacitors is then impossible so that the input pulses are always based on zero potential.

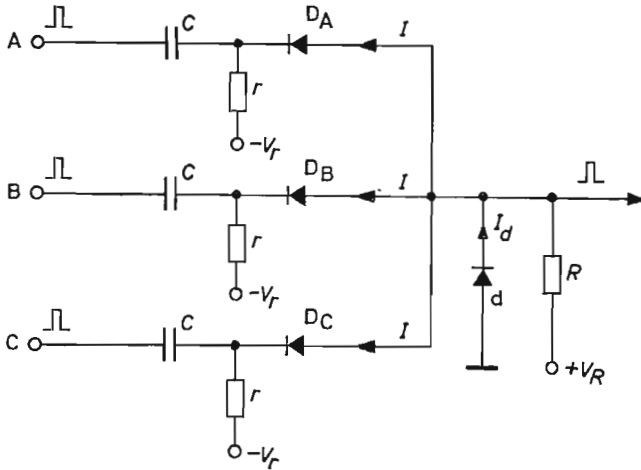


Fig. 4.16 And-gate capacitively coupled

If there is no positive voltage at any of the n inputs, the current through the diode d is

$$I_d = n \frac{V_r}{r} - \frac{V_R}{R} \quad (4.5)$$

while the load current of the input diodes is

$$I = \frac{V_r}{r}$$

The necessary blocking voltage of the input diode is given by the amplitude of the input voltages, the blocking voltage of diode d by the voltage V_R . In the case of coincidence, the blocking resistances $R_{s\text{ inv}}$ of the diode lie parallel to the working resistance R . With And-gates with n inputs, the condition

$$\frac{R_{s\text{ inv}}}{n} \gg R \quad (4.6)$$

must be valid so that the complete voltage appears at the output. Referring to Equation (4.2), this means that diodes with a large blocking-transmission ratio are suitable for gates with many inputs.

4.1.3.3 And-gate with transistors

Once again we obtain the And-gate from the Or-gate (Fig. 4.11) by exchanging the rest and working conditions. If all the transistors are opened in the rest condition through an appropriate base voltage V_{BEX} , a pulse is only obtained at the output if all the inputs are blocked by V_{BEY} . This circuit also causes a simultaneous change of polarity of the input pulses.

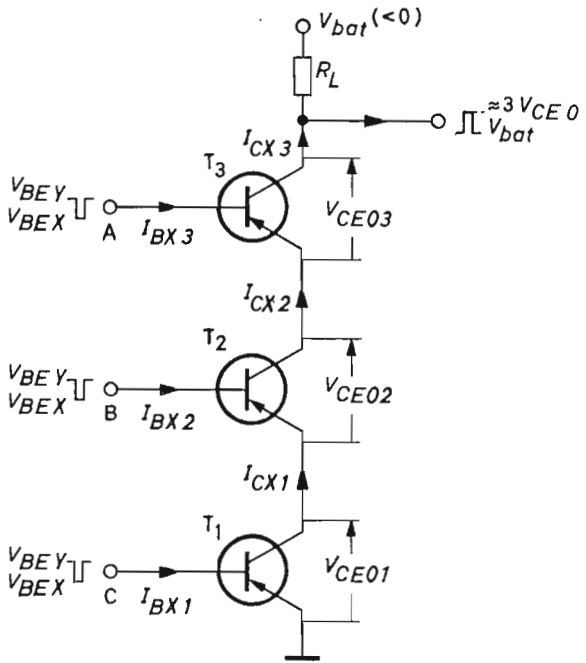


Fig. 4.17 And-gate in series circuit

In the rest condition, with a circuit of this type, the opening current I_{CX} flows through each transistor. In gates with many inputs the feed voltage source is thus comparatively heavily loaded. A circuit can now be constructed which does not possess this disadvantage and for which there is no analogous tube circuit. The And-gate shown in Fig. 4.17 consumes practically no current in the rest condition, and only the opening current of a transistor in the case of coincidence when all the inputs are addressed. It is an important property of this circuit that the input voltages of all the transistors can move at the same level although the transistors are all connected in series, since the sum of the residual voltages is small. Experience shows that we can construct reliable gates in this way with up to five inputs. It is necessary to ensure here that the collector currents of the individual transistors are different, as the base current is added from stage to stage. Thus, as an example, the collector current of transistor T_1 is:

$$I_{CX1} = I_{CX3} + I_{BX2} + I_{BX3}$$

In this case the base currents are reduced from stage to stage on account of the voltage drop at the transistors:

$$|I_{BX1}| > |I_{BX2}| > |I_{BX3}|$$

The lower transistors are thus more controlled than the upper ones.

The circuit for a capacitively-coupled And-gate is shown in Fig. 4.18 [53].

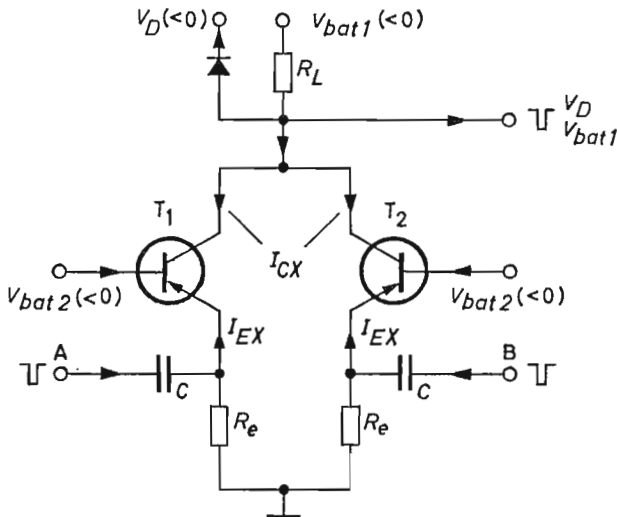


Fig. 4.18 Capacitively coupled And-gate

The two transistors are controlled here via their external emitter resistance so that the output pulses retain the polarity of the input pulses. In the rest condition, both transistors are conducting. The load resistance R_L and the bias V_D of the diode are chosen so that

$$|V_{bat1} - I_{CX} R_L| < |V_D|$$

Then the diode keeps the voltage at the output of the gate at V_D , no matter whether both transistors are opened, or only one. The output voltage only drops to V_{bat1} if both transistors are blocked through negative pulses at A and B, since now the diode has also become currentless. The voltage V_{bat2} is chosen so that

$$V_{bat2} = V_{BEX} - I_E R_e$$

when V_{BEX} is the opening voltage necessary at the base. The blocking occurs through pulses which make the emitter more negative by the base blocking voltage V_{BEX} , in comparison with the base.

In order to send clock pulses either along line I or line II, according to the position of a bistable multivibrator (Fig. 4.19), we can use two And-gates controlled from the output voltages of the bistable multivibrator M. We can, however, also combine the two And-gates into a common gate with two outputs, as is shown in Fig. 4.20 [53]. The two inputs B_1 and B_2 are connected with the outputs of the bistable multivibrator, input A being fed from the clock pulses. Without input pulses, T_1 is blocked (through the leakage resistance R_{be}). Outputs I and II then lie at V_{bat} independent of the voltages at B_1 and B_2 . If a negative pulse occurs at input A, the emitters of T_2 and

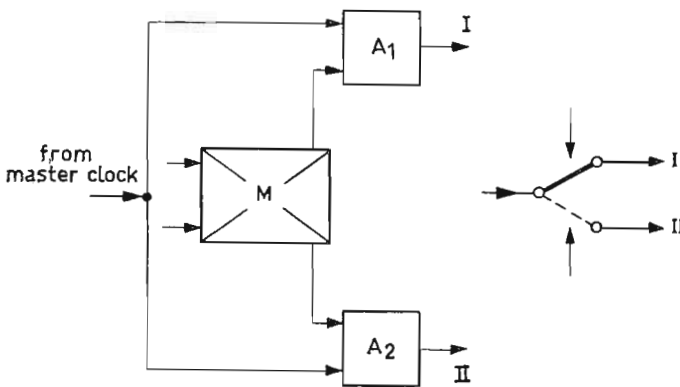


Fig. 4.19 Change-over switch for the master-clock pulses

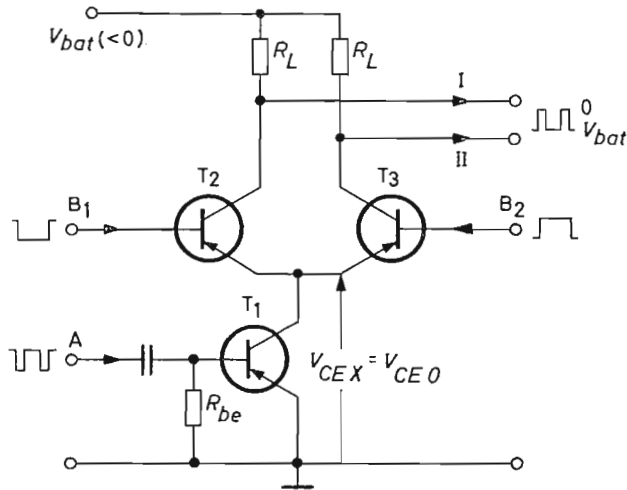


Fig. 4.20 Double And-gate as change-over switch

T_3 are at the residual voltage V_{CE0} of transistor T_1 . If the high (positive) voltage of the multivibrator is $> V_{CEX}$, it blocks the corresponding transistor, e.g. T_3 , while its low voltage keeps transistor T_2 open in so far as it lies about V_{BEX} below the residual voltage V_{CE0} . Then a pulse only appears at output I because here the voltage rises from V_{bat} to zero while it remains at V_{bat} at output II. Base voltages below 1 V are sufficient for control.

4.2 Bistable and monostable flip-flop circuits

Static and dynamic behaviour are important criteria for the suitability of a flip-flop circuit (compare Section 2.4.2), as well as its power consumption and space requirements in view of the great number used in computers.

The *static* operation determines the stability of the circuit and the height of the voltage jump at the output. Working reliability requires the circuit to be as resistant as possible to disturbances (fluctuations of the feed voltages and disturbing pulses from adjacent switch circuits) and to specimen scattering and ageing of the components used. Great stability is maintained by the use of high-value components with low spreads and by making sure, through suitable circuit dimensioning, that the input voltages at the blocked systems lie sufficiently below the corresponding blocking voltages.

The sensitivity, the duration of switch-over and the maximum switch frequency depend on the *dynamic behaviour*. The sensitivity is given by the value of the pulse necessary for reliable switch-over and depends not only on the circuit itself but also on the kind of coupling to the triggering source.

The *switch-over* of the two conditions of a bistable flip-flop circuit can take place in different ways: First, trigger pulses are sent to both inputs via separate control lines; second, the inputs can also be coupled in a suitable way to a common control line. In case a of Fig. 4.21, each control line is coordinated to a certain condition of the multivibrator. A pulse along control line I, for example, always produces the even condition of the multivibrator, and along control line II, the odd condition. If the multivibrator is already in the even condition, a pulse on line I produces no alteration. An arrangement of this kind is always used where the multivibrator is to be controlled from two different sources, as is the case in many switch and storage tasks. Case b, on the other hand, switch-over via a control line, takes place when the multivibrator is used as a reducer in counter circuits. In this case the condition of the multivibrator must change after every pulse at the input.

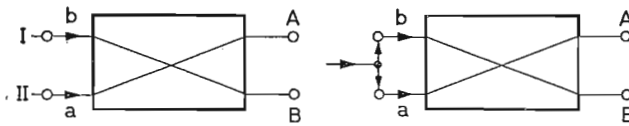


Fig. 4.21 Switch-over of the bistable multivibrator

- awith separate control lines
 bwith common control line

By appropriately uncoupling the inputs we can ensure that each pulse arriving is only effective at one input, namely the one appropriate for switching over from this condition. Since the inputs are at different voltages, according to the condition of the multivibrator, this can be achieved, for instance, with diodes at bias potential.

The *period of switch-over* of a flip-flop circuit depends on the active components used (tubes, transistors, square-loop ferrite cores), the dimensioning of the circuit and the value, duration and form of the release pulse. Its duration should roughly correspond to the switch-period. If the release pulse is too short, triggering either does not occur at all, or is too slow; if it is too long, the recovery time of the circuit is protracted.

In the main, multivibrators consist of vacuum tubes and transistors, and the method of coupling is the chief difference between the two systems. The advantage of cathode- or emitter-coupled circuits is that the triggering process is only insignificantly affected by the internal resistance of the release source or the associated load. Anode- or collector-coupled circuits, on the other hand, are sensitive in this respect, though their stability and dynamic behaviour are more favourable.

4.2.1 TUBE CIRCUITS

4.2.1.1 Anode-coupled bistable multivibrator

Bistable multivibrators can be constructed with triodes and multigrid tubes. Double triodes are almost exclusively used in computer construction. Fig. 4.22 shows the basic circuit diagram of a symmetric arrangement. Apart from the automatic generation of grid bias through cathode resistance R_k which is used here, we can also work with a fixed bias. On account of the counter coupling through R_k , this circuit is more stable, however, in the face of slow disturbances and fluctuations of the feed voltage. As well as the capacitors C and C_k built into the circuit, the harmful parallel capacitances C_1 and C_2 , effective at the tube inputs and outputs, are also marked; these consist of the input- or output capacitance of the tubes and the switch capacitance.

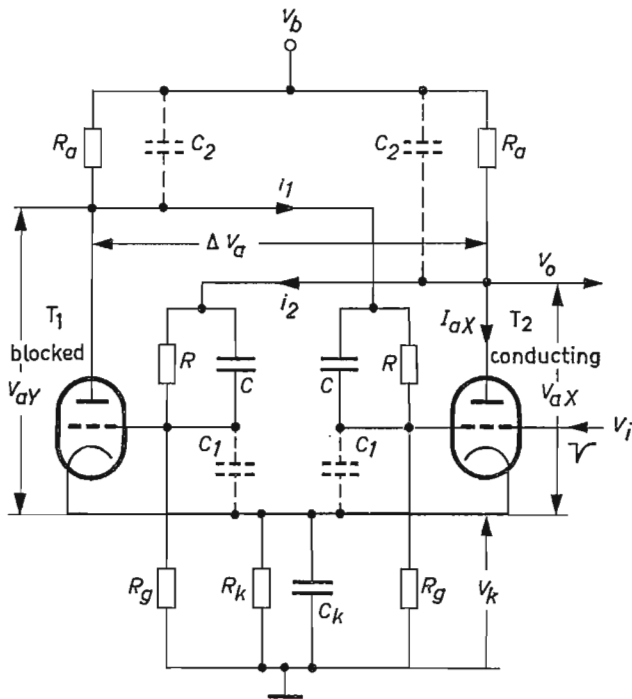


Fig. 4.22 Basic circuit of the bistable multivibrator

The circuit is thus characterised by the fact that only one of the two tubes is conducting at a time. These conditions are stable with suitable choice of component values, because, as a result of the counter-coupling of the two

tubes via resistances R , the low anode voltage of the conducting tube 2 constantly blocks the currentless tube 1, while the high anode voltage of tube 1 keeps tube 2 open, and vice versa.

The static ratios are determined by the voltage dividers formed by the tubes and resistances. The dynamic properties govern the processes of triggering over from one stable condition to the other, brought about by a suitable release pulse. They depend chiefly on the properties of the types of tubes in use, on the capacitor C and the harmful parallel capacitances C_1 and C_2 . Furthermore, the stability of the circuit against changes (interfering pulses, signs of ageing and component spreads) also plays a part. The outline of the circuit is based on the static and dynamic processes, and we shall concern ourselves first with the dynamic behaviour. This describes the characteristic properties of the circuit and also influences the static dimensioning.

Dynamic behaviour:

The theoretical treatment of the trigger process is laborious [43] and not very clear, so we shall content ourselves here with approximate considerations. We assume in this case that the cathode capacitor C_k is so big that the time constant $R_k C_k$ is longer than the triggering process; the voltage at the cathode resistance then remains approximately constant during triggering.

We then proceed on the assumption that the bistable multivibrator shown in Fig. 4.22 is released by a negative pulse V_i with steep front edge and flat rear edge, at the grid of the opened tube (T_2), its amplitude being greater than the blocking voltage of the tube. We can then differentiate between the following periods:

- $\tau_1 \dots$ grid voltage of tube 2 reaches the blocking voltage $V_{g \text{ inv}}$
- $\tau_2 \dots$ anode voltage of tube 2 rises to the stationary value V_{aY}
- $\tau_3 \dots$ grid voltage of tube 1 rises from V_{gY} (the grid voltage jump) to zero value
- $\tau_4 \dots$ anode voltage of tube 1 drops to the stationary value V_{aX}
- $\tau_5 \dots$ grid voltage of tube 2 reaches the stationary value V_{gY} .

These processes are shown qualitatively in Fig. 4.23. Provided there is a sufficiently steep release pulse, the first section τ_1 can be ignored. The rise of the anode voltage of tube 2 is then determined solely by the time constant effective at the anode, formed by the RC section shown in Fig. 4.24. The anode current I_{aX} and the internal resistance r_{aL} are suddenly switched off by the blocking of the tube. The anode voltage v_{a2} and the grid voltage v_{g1}

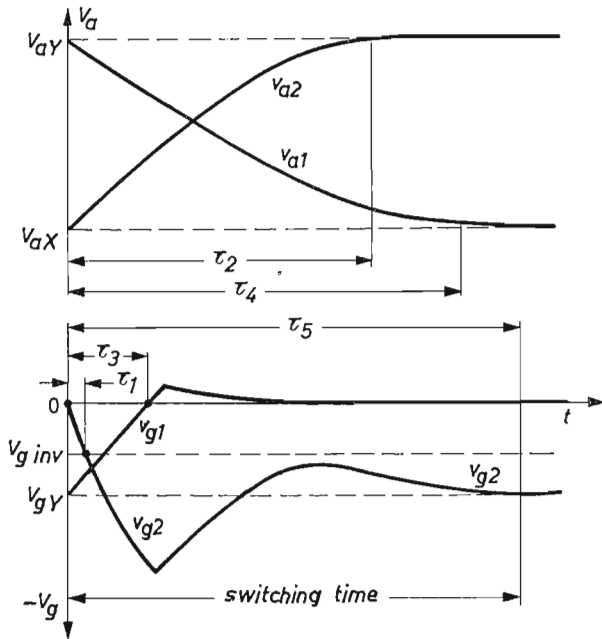


Fig. 4.23 Grid and anode voltages during triggering

can then be calculated [44]; here we shall content ourselves with an evaluation.

Provided that

$$\left. \begin{matrix} R_g C_1 \\ RC \end{matrix} \right\} > R_a C_2 \tag{4.7}$$

holds good for the time constant, the grid voltage v_{g1} in the first instance approximately follows the anode voltage v_{a2} reduced by the factor $C/C + C_1$:

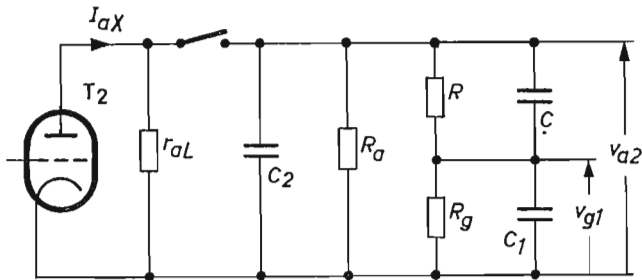


Fig. 4.24 Circuit at the anode of tube 2

$$v_{g1} \approx \frac{C}{C + C_1} \times v_{a2} \quad (4.8)$$

So that tube 1 is fully opened as quickly as possible, it is essential that

$$C \gg C_1 \quad (4.9)$$

The anode voltage v_{a2} itself, according to condition (4.7) above, proceeds approximately with the time constant formed by the parallel circuit of resistances R_a and $R_g + R$ and the capacitances C_2 and $C + C_1$. After instant τ_3 , however, where v_{g1} has become equal to 0, the grid current of tube 1 counteracts the overswing of the grid voltage, i.e. capacitor C is now practically earthed so that now the time constant

$$T_{rise} = \frac{R_a R}{R_a + R} (C + C_2) \quad (4.10)$$

is effective at the anode. If we introduce the anode voltage jump ΔV_a , we then have

$$T_{rise} = \frac{1}{\frac{I_{aX}}{\Delta V_a} + \frac{1}{R}} (C + C_2) \quad (4.11)$$

As soon as $v_{g1} = 0$, the anode voltage v_{a1} has approximately the time constant

$$T_{fall} = \frac{R_a r_{aL}}{R_a + r_{aL}} \left(C_2 + \frac{C C_1}{C + C_1} \right) \quad (4.12)$$

where r_{aL} is the internal resistance of the opened tube 1. The quicker v_{g1} reaches zero value (small τ_3) and the smaller T_{fall} is, the more rapid will be the drop of the anode voltage. The first condition is then fulfilled through a large capacitor C (according to (4.9)). A large value of C , however, impairs the time constants of both pulse edges (compare Equations (4.11) and (4.12)) and again lengthens time τ_3 because of Relation (4.8). In practice we choose C to be about equal to the effective output capacitance C_2 (about 10 to 50 pF).

The course of the grid voltage v_{g2} is obtained by superimposing the trigger pulse on the reverse-coupled voltage from the anode of tube 1. At first the trigger pulse prevails. After its cessation the reverse-coupled voltage alone remains, v_{g2} now running according to the time constant

$$T_g = RC \frac{R_g(R_a + r_{aL}) + R_a r_{aL}}{(R + R_g)(R_a + r_{aL}) + R_a r_{aL}} \quad (4.13)$$

Fresh triggering of the multivibrator is generally only possible when all the voltages and currents have almost reached their stationary end values. This period thus determines the maximum switching frequency. For the complete recovery time of the circuit we can estimate approximately

$$\tau_5 = (2 \text{ to } 3) T_g$$

Since the value of C is established by Relation (4.9), it also follows from Equations (4.12) and (4.13) that small values of R , R_a and r_{aL} are necessary for high switching frequencies.

The cathode capacitor C_k limits the counter-coupling through the cathode resistance towards higher frequencies and thus reduces the resistance of the circuit to steep interfering pulses. On the other hand, the voltage across R_k should remain constant during the triggering process so that

$$R_k C_k > \tau_5$$

Static behaviour:

The d.c. behaviour of the circuit is determined by the type of tube used and the resistances, and can be calculated by means of Kirchoff's laws. We find the following relations [44]:

$$\frac{R}{R_g} = \frac{\Delta V_a}{V_{gY}} - 1 \quad (4.14)$$

$$R_g = \frac{V_{gY}}{I_{aX}} \times \frac{1}{1 - \left(1 + \frac{R_g}{R}\right) \frac{V_{aY}}{V_b}} \quad (4.15)$$

$$R_a = \frac{1}{1 + \frac{R_g}{R}} \times \frac{\Delta V_a}{I_{aX}} \times \frac{V_b}{V_{aY}} \quad (4.16)$$

$$R_k = \frac{R_g}{R} \times \frac{V_{aY}}{I_{aX}} \quad (4.17)$$

The symbols here signify:

ΔV_a . . . anode voltage	}	between blocked and opened conditions of the tubes
change		
V_{gY} . . . grid voltage	}	between blocked and opened conditions of the tubes
change		
I_{aX} . . . anode current with opened tube		
V_{aY} . . . anode voltage of blocked tube		
V_b . . . feed voltage		

Presuming that the d.c. resistance of the opened tube is constant (because $V_g = 0$, we find ourselves in the limiting characteristic r_{aL} in the I_a/V_g static curves), the circuit of Fig. 4.22 represents a linear network in the stable condition, i.e. all the currents and voltages are proportional to the feed voltage V_b . Since the values of the resistances depend merely on the ratio V_{aY}/V_b , and not on the feed voltage V_b alone, this means that the choice of resistances is independent of V_b . The circuit working with a cathode resistance is thus more stable in the stationary condition than a circuit with fixed cathode bias V_k . Four of the eight values included are established by Equations (4.14) to (4.17). We thus still have four values to choose, with which we can adjust the circuit optimally to its purpose. So that the resistances do not become negative, we must also see that

$$\frac{V_{gY}}{\Delta V_a} < 1 \quad \text{and} \quad \frac{V_{aX}}{V_b} < 1 - \frac{V_{gY}}{\Delta V_a} \quad (4.18)$$

Selection of tube types:

To achieve a short switch-over period and great sensitivity of the circuit, the grid voltage change V_{gY} must be as small as possible, as is evident from Fig. 4.23. This calls for tubes with small blocking voltage $V_{g \text{ inv}}$: The smaller this is, the faster are both tubes controlled and the shorter are the switching and recovery times of the bistable multivibrator. The blocking voltage increases as a result of the reciprocal of the amplification factor roughly in proportion to the anode voltage of the tube (see Equation (3.5)). To achieve a small blocking voltage we thus need tubes with large amplification factor and low anode voltage at the blocked tube. This amounts to

$$V_{aY} = (V_{aX} + \Delta V_a) \approx I_{aX} (r_{aL} + R_a)$$

i.e. with given values for I_{aX} and R_a , the internal resistance r_{aL} must have a low value.

For short output rise or falling times, we need, according to (4.11) and

(4.12), small parallel capacitances and a large anode current I_{aX} , as well as a small r_{aL} . Altogether, we thus require tubes with large anode current, large amplification factor, small internal resistance and low capacitances. With the exception of the capacitances, these values for different double triodes are contained in Table 3.1. Since the anode leakage capacitance of the circuit at given values of ΔV_a and R_a is proportional to r_{aL} , tubes with small r_{aL} are preferable to tubes with large μ in view of the energy consumption and the heating of the equipment. The tube capacitances are not of very great importance since they are usually covered by the switching capacitances and other load capacitances.

Outline of the circuit:

As a rule, the value of the anode voltage jump ΔV_a and either the switching times or the maximum switching frequency will be prescribed.

From the circuit in Fig. 4.22, we have for the anode current

$$I_{aX} = \frac{\Delta V_a}{R_a} + (i_1 - i_2)$$

where the difference of the voltage divider currents i_1 and i_2 is not yet known. Since this only amounts to a fraction of the current $\Delta V_a/R_a$, an estimate is sufficient here since experience shows that

$$I_{aX} \approx (1.1 \text{ to } 1.2) \frac{\Delta V_a}{R_a} \quad (4.19)$$

Since in the first approximation

$$C = C_2 \text{ and } R > R_a$$

it follows from Equation (4.11) that the time constant

$$T_{an} \approx 2 R_a C_2 \quad (4.20)$$

If we require a short switching time, we can estimate the value of R_a from Equation (4.20). The necessary anode current is then derived from the desired output voltage ΔV_a . For slowly operating circuits, on the other hand, we can assume I_{aX} and determine R_a from Equation (4.19).

We can now select the appropriate tube with this anode current from Table 3.1; thus for rapid circuits, a tube with small reciprocal of the amplification factor and small r_{aL} . In the I_a/V_a characteristic curves, as Fig. 4.25 shows, the straight line of resistance $R_a/(1.1 \text{ to } 1.2)$ can be plotted at point X

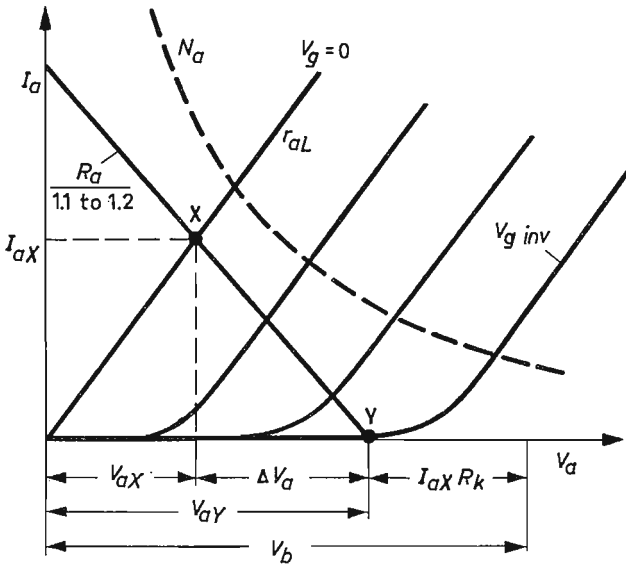


Fig. 4.25 I_a/V_g characteristic areas for determining $V_{g \text{ inv}}$

given by I_{aX} on the limiting characteristic line r_{aL} , and from point Y we obtain the blocking voltage $V_{g \text{ inv}}$ of the tube.

From the blocking voltage $V_{g \text{ inv}}$ we get the minimum value of the required grid voltage change V_{gY} . For reasons of stability V_{gY} should be sufficiently greater than $V_{g \text{ inv}}$. On the other hand, the dynamic behaviour of the circuit is impaired by a large value of V_{gY} because of its strong influence on τ_3 . In general we put

$$V_{gY} = k V_{g \text{ inv}} \quad (4.21)$$

in which the factor k usually lies somewhere between 1.5 and 2. We now select the values for C and R from the Relations (4.9) and (4.7). Thus, of the nine values of Equations (4.14) to (4.17) only the resistances R_g and R_k and the feed voltage V_b are still unknown. We estimate resistance R_g from (4.14), R_k from (4.17) and the feed voltage (compare Fig. 4.25) from

$$V_b \approx I_{aX} (r_{aL} + R_k) + \Delta V_a \quad (4.22)$$

Initiating the triggering process:

The bistable multivibrator can be switched over by pulses of suitable polarity at the anodes, the grids or the cathodes. We have to distinguish therefore,

as mentioned earlier, whether the initial triggering should occur for both positions over one input lead, as, for instance, in counter circuits, or over two leads for one condition at a time. A suitable decoupling must be provided to prevent the internal resistance of the source of the trigger pulses affecting the circuit. The simplest method is to couple the trigger pulses over small capacitors which do not raise the capacitances of the circuit to any great extent. A more favourable separation can be achieved in many cases by suitably biased diodes. As soon as the grid voltage falls below a certain value, the trigger source is switched off.

Fig. 4.26 shows three possibilities for triggering over one input. Either the trigger pulses operate at a common anode resistance R_A (a) or at a common cathode resistance R_K (b) or they are led to the two grids (c.) Since in case (c) the blocked tube also receives a negative pulse, the triggering is impeded, particularly at high frequencies. We maintain more favourable conditions by including diodes which only transmit one trigger pulse at a time to the conducting tube.

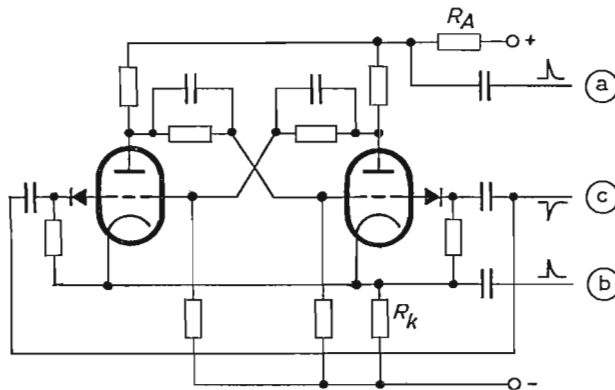


Fig. 4.26 Triggering arrangements of the bistable multivibrator

The size, form and duration of the trigger pulse influence the triggering process and the maximum switching frequency, as has already been illustrated in Fig. 4.23. The leading edge should be as steep as possible while the rear edge must run flat to avoid back triggering through possible differentiation. With high switching frequencies the duration of the pulse must not be so long that period τ_5 is protracted. Its half-width value should then correspond to about T_{ab} according to equation (4.12). Finally, the amplitude of the release pulse is not too great for the same reason.

Working reliability of the bistable multivibrator:

The stability of the circuit can be impaired by external disturbing influences (voltage fluctuations, disturbing pulses), by ageing of the tubes, resistance changes and spreads in the components used. Stability criteria can be drawn up by selecting the most unfavourable combinations of the permissible resistance and tube spreads (production spreads and during life) and checking the behaviour of the circuit. It is most sensitive to grid voltage fluctuations. The effect of resistance deviations on the conditions of conducting and blocked tubes, as well as the influence of interfering pulses are investigated in [45]. By using bistable multivibrators in counter circuits we find that with normal design of the circuit, the tolerances for the resistances can amount to $\pm 20\%$ [46].

Examples of circuits:

Fig. 4.27 shows an example of a bistable multivibrator constructed with tube E 92 CC [47]. Triggering takes place with about -20 V at both grids; the maximum switching frequency amounts to 1 Mc/s. The anode voltage jump lies at 40 V, its rise time being about 0.2 μ s.

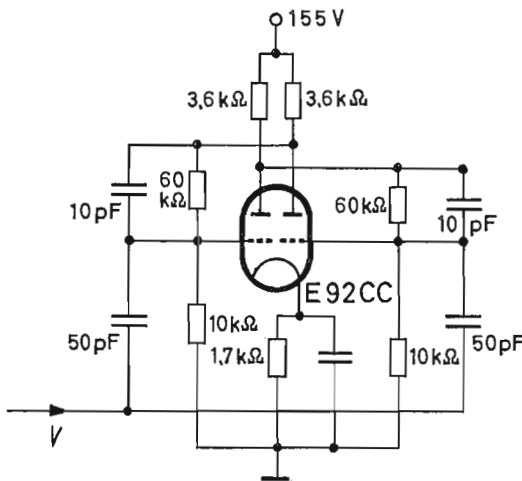


Fig. 4.27 Circuit with the double triode E 92 CC

A further circuit using tube E 90 CC [45] is shown in Fig. 4.28. Triggering occurs over a common input through a negative pulse at both anodes; these are decoupled through the two diodes D_1 and D_2 . By introducing resistance

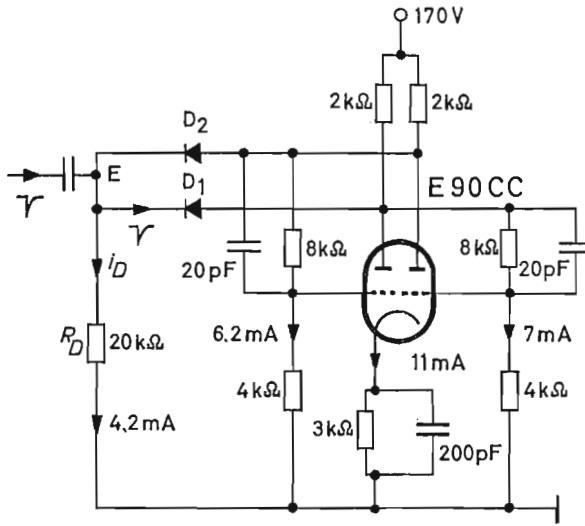


Fig. 4.28 Circuit with the double triode E 90 CC

R_D , the diodes become parts of a voltage divider. Then only the diode at the grid of the conducting tube transmits the release pulse. The current of this diode supplies in E the voltage V_{aX} , so that D_2 is blocked because of the lower anode voltage V_{aX} of the conducting tube. The cross current i_D has to be taken into consideration in the static design. The switching time of this circuit amounts to 65 ns with which counting frequencies up to about 14 Mc/s can be reached with about 20 V output voltage.

Indication of condition:

In some cases a visible indication of the condition of a bistable circuit is desirable. This can be obtained with neon lamps, measuring instruments or indicator tubes. When a neon lamp is used it is placed across a series resistor between anode and cathode of for instance, tube 1 (Fig. 4.22). It then gives an indication with tube 1 blocked. It is a condition for this that the anode voltage jump is greater than the difference between the ignition- and burning voltages of the neon lamps used. This requirement cannot be fulfilled with high switching frequencies. Indicator tubes can then be used with advantage.

Tube DM 160 is well suited for this since it only needs a grid voltage of about 3 V to control its fluorescent screen. As Fig. 4.29 shows, grid and anode of the indicator tube are each connected via a resistance parallel to the voltage divider resistance R . There is then an indication at the fluorescent

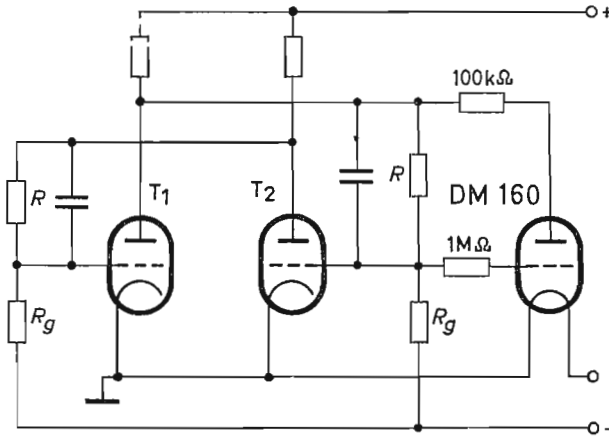


Fig. 4.29 Indication of condition with the indicator tube DM 160

screen when tube 1 is blocked and tube 2 is conducting, since the grid of the indicator tube is then at zero voltage.

4.2.1.2 Cathode-coupled bistable multivibrator (Schmitt-Trigger)

By omitting the coupling between anode and grid and introducing a common unbypassed cathode resistance which takes over the feedback, we obtain the circuit of Fig. 4.30 from the one shown in Fig. 4.22. It offers the advantage that the grid at which the trigger pulses are applied and the anode at which the output pulses are tapped are not directly concerned with the feedback,

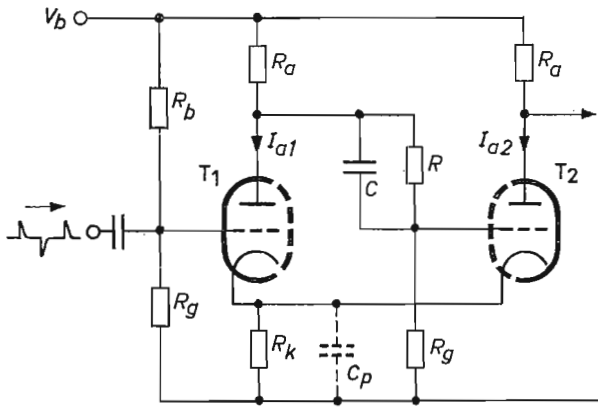


Fig. 4.30 Principle of the Schmitt-trigger

so that the internal resistance of the trigger source and the output load do not appreciably affect the triggering process. The circuit (with only one input) must be released alternately with positive and negative pulses according to the stable condition.

We shall assume that the left tube is blocked and the right one is conducting. This condition is stable since the anode current I_{a2} keeps tube 1 blocked via the cathode resistance. The circuit is triggered over through a positive pulse at the grid of tube 1; tube 1 is now opened and tube 2 blocked. The current I_{a1} which appears in this position is less than I_{a2} . This condition is also stable since T_2 is additionally blocked by the voltage drop at R_a .

This multivibrator can thus be triggered to-and-fro by release pulses of changing polarity. A further use of this circuit is the generation of a square wave voltage from any chosen alternating voltage as is shown in Fig. 4.31.

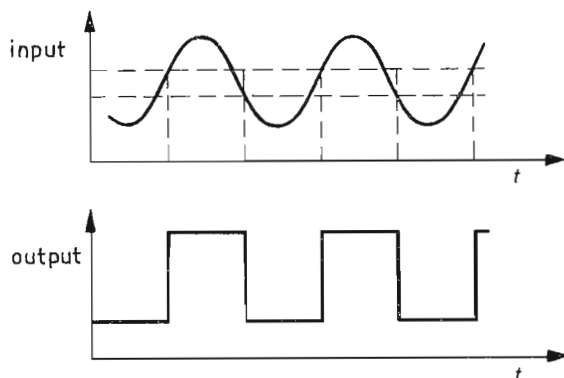


Fig. 4.31 Production of a square-wave voltage with the Schmitt-trigger

Each time the input voltage exceeds a certain threshold value, the multivibrator triggers over and yields at its output a square wave voltage which is largely independent of the form of the input voltage.

The approximate calculation of the circuit can be carried out in a simple manner: We proceed on the assumption that the anode voltage V_{a2} of tube 2 and the working resistance R_a (stipulated by the necessary flank steepness) are already given. Then, for the anode current required,

$$I_{a2} = \frac{\Delta V_{a2}}{R_a}$$

and we can select a suitable tube. We now establish the anode current which tube 1 carries in the conducting condition, and we choose I_{a1} about 10% less than I_{a2} :

$$I_{a1} \approx 0.9 I_{a2} \quad (4.23)$$

The cathode voltage of tube 1 is then

$$V_k = I_{a1} R_k \quad (4.24)$$

and the grid voltage difference compared with the blocked condition is

$$V_{gY1} = (I_{a2} - I_{a1}) R_k \quad (4.25)$$

From the I_a/V_a characteristic curve (Fig. 4.32) we can find at point Y the blocking voltage $V_{g \text{ inv}}$ of tube 2 which also corresponds to the blocking voltage of tube 1. With the safety factor k (according to (4.21)), we can thus set down for both grid voltage jumps

$$V_{gY1} = V_{gY2} = k V_{g \text{ inv}} \quad (4.26)$$

From (4.25) the cathode resistance is

$$R_k = \frac{V_{gY1}}{I_{a2} - I_{a1}}$$

and the feed voltage V_b is then derived from

$$V_b = I_{a2} (R_a + r_{aL} + R_k)$$

We thus obtain from the characteristic curve (point X) the grid voltage V_{g1}

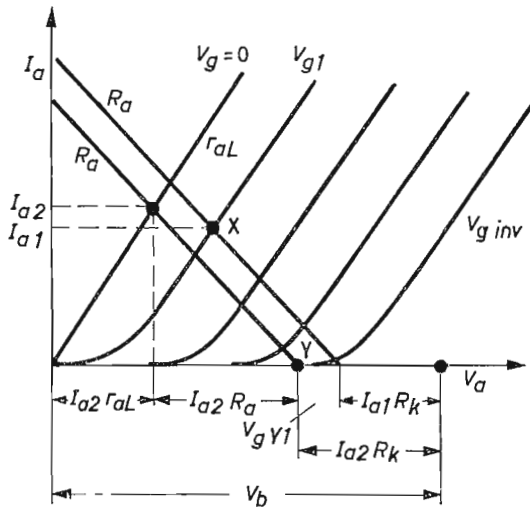


Fig. 4.32 I_a/V_a characteristic curves for calculating the Schmitt-trigger

in the conducting condition of tube 1. Finally, when tube 2 is blocked, the grid voltage jump is:

$$V_{gY2} = k V_{g \text{ inv}} = I_{a1} R_a \frac{1}{1 + R/R_g} - V_{gY1}$$

from which the ratio of the voltage divider resistances is obtained:

$$\frac{R}{R_g} = \frac{I_{a1} R_a}{2 k V_{g \text{ inv}}} - 1 \quad (4.27)$$

The choice of R (and of C) can thus be made from the same viewpoints as in the bistable circuit, according to Relations (4.9) and (4.7) so that we can estimate R_g from Equation (4.27).

The grid voltage V_{g1} of the conducting tube 1 consists of the difference of the cathode voltage (4.24) and the fixed positive grid bias obtained through voltage division:

$$V_{g1} = I_{a1} R_k - V_b \frac{R_g}{R_g + R_b}$$

so that we can now calculate the missing voltage divider resistance R_b :

$$R_b = R_g \frac{V_b + V_{g1} - I_{a1} R_k}{I_{a1} R_k - V_{g1}} \quad (4.28)$$

The same considerations apply for the dynamic behaviour as in Section 4.2.1.1. In essential, the flanks of the output pulse are determined here by the time constant operating at the anode of tube 2; they therefore proceed according to Equations (3.2) and (3.4). The recovery time of the circuit, and thus its maximum switching frequency, depends here on the time constants $R_k C_p$ operating at the cathode which, in consideration of the cathode resistance implied in Equation (4.25), cannot be kept as small as is desirable. (C_p corresponds in principle to the single or double cathode-to-heater capacitance C_{fk} , according to whether the double triode has common or separated cathodes). The greater the difference between the anode currents $I_{a2} - I_{a1}$, the more favourable is the recovery time of the circuit. On the other hand, a small value of I_{a1} spoils the switching times since there is then less voltage available for the control of tube 2. By appropriate choice of Equation (4.23) it is thus in our hands to balance maximum switching frequency and flank steepness of the output pulse one against the other.

4.2.1.3 Anode-coupled monostable multivibrator

The basic circuit of the monostable multivibrator shown in Fig. 4.33 is

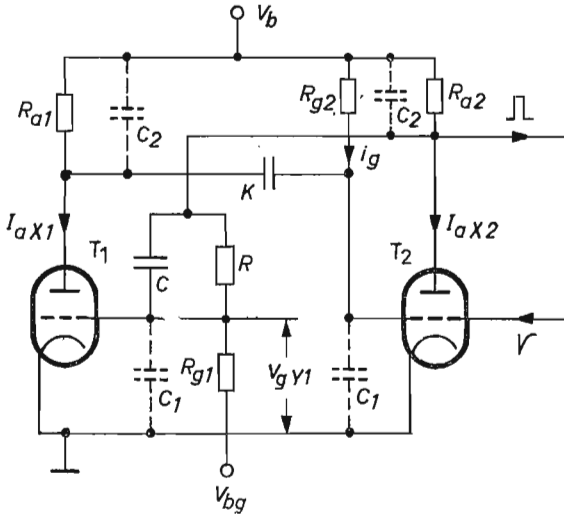


Fig. 4.33 Anode-coupled monostable multivibrator

obtained from the bistable circuit (Fig. 4.22) by substituting the direct coupling, e.g. from the anode of tube 1 to the grid of tube 2, by a purely capacitive coupling with the coupling capacitor K . Since the resistances are frequently different in this circuit, we also use here for expedience a fixed grid bias for tube 1 (so as to be independent of the pulse frequency).

In the rest condition of the circuit, tube 2 is conducting and tube 1 blocked. The grid voltage v_{g2} is thus produced at the leakage resistance through the grid current and lies at about zero so that for the grid current we obtain approximately

$$i_g \approx \frac{V_b}{R_{g2}}$$

Fig. 4.34 shows the course of the voltage at the grids and anodes when the circuit is released by a sufficiently steep negative pulse at the conducting tube 2. After time τ_1 tube 2 is blocked; its anode voltage v_{a2} rises from $I_{a2}r_{aL}$ by the voltage jump

$$\Delta V_{a2} = I_{a2} R_a \left(1 - \frac{i_{2Y} - i_{2X}}{I_{a2}} \right) \approx I_{a2} R_a \quad (4.29)$$

when $i_{2Y} - i_{2X}$ is the difference of the voltage divider currents in the conducting and blocked conditions of tube 2. Here the flank runs in complete accordance with the triggering process in the bistable multivibrator, thus ap-

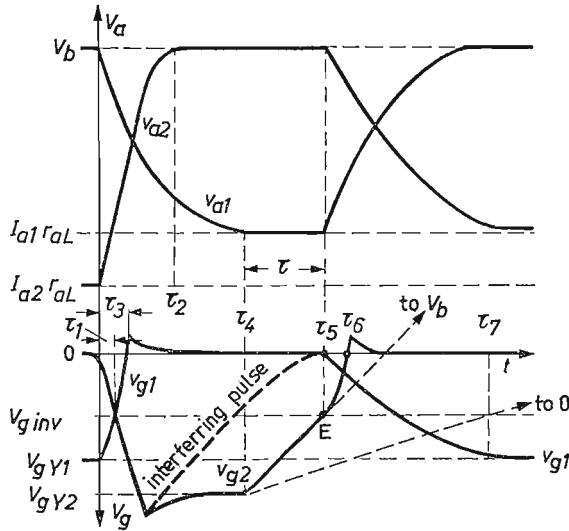


Fig. 4.34 Grid and anode voltages during triggering of the bistable multivibrator

proximately with the time constant T_{rise2} , according to (4.10). At the same time the anode voltage of tube 1 begins to drop from instant τ_3 when $v_{g1} = 0$, v_{a1} falling with the time constant T_{fall1} according to Equation (4.12) to the value $I_{a1} r_{aL}$. The grid voltage v_{g2} of tube 2 approximately follows the anode voltage v_{a1} via the coupling capacitor K as soon as the release pulse has ceased to operate. If v_{a1} has reached the end value $I_{a1} r_{aL}$ (at instant τ_1) the coupling capacitor begins to discharge over its leakage resistance R_{g2} , towards voltage V_b . If, at instant τ_5 , the grid voltage v_{g2} exceeds the blocking voltage $V_{g\text{ inv}}$ (point E), the feedback of the circuit commences; it triggers back. The decreasing anode voltage of tube 2 starts to block tube 1 again and the rising anode voltage of this tube in its turn again raises the grid voltage of tube 2. In this way zero grid voltage is reached comparatively quickly (τ_6). Now the anode voltage v_{a1} rises with the time constant according to Equation (4.10) to the feed voltage V_b while v_{a2} drops with the time constant T_{fall2} according to Equation (4.12). The triggering process is thus completed when the grid voltage v_{g1} has reached its stationary value V_{gY1} .

As well as the time constants of the anode voltage flanks given by Equations (4.10) and (4.12), the rest time τ in the quasi-stationary condition is also of interest in monostable multivibrators. In essential it is given through the time constant $R_{g2} K$. The grid voltage runs as far as point E (period τ_5) according to the recharging of the coupling capacitor from voltage V_{gY2} to V_b .

Since $\tau_5 - \tau_4 = \tau < R_{g2}K$, we obtain for the rest time approximately

$$\tau = R_{g2}K \frac{I_{a1} R_{a1} - V_{g \text{ inv}}}{V_b + I_{a1} R_{a1}} \quad (4.30)$$

We now also see why it is more convenient to apply R_{g2} at the feed voltage and not at the cathode, as the point of intersection E' illustrates in Fig. 4.34. The voltage v_{g2} would cut the blocking voltage substantially flatter so that the rest time would be much more dependent on fluctuations and interfering pulses. As long as we can regard the stationary circuit as linear, τ is not dependent on V_b since I_{a1} and $V_{g \text{ inv}}$ in (4.30) are proportional to V_b .

The recovery time of the circuit, τ_7 , is made up of the rest time τ and the rise or falling time.

The design of the circuit is similar to that of the bistable multivibrator. Here we only obtain a relation for the ratio of resistances R and R_{g1} :

$$R/R_{g1} = \frac{I_{a2} r_{aL} + V_{gY1}}{V_{bg} - V_{gY1}} \quad (4.31)$$

We thus have a greater degree of freedom here so that R and V_b , for example, are still open to choice.

The statements concerning starts of the triggering process in the bistable multivibrator are also valid here. When monostable multivibrators are used as delay elements, it is especially important to note that the trigger process and therefore the delay time also are governed by the form and size of the release pulse [48].

4.2.1.4 Cathode-coupled monostable multivibrator

Analogous to the Schmitt-Trigger (see Section 4.2.1.2), we obtain the cathode-coupled monostable multivibrator by omitting the direct coupling shown in Fig. 4.33, between the anode of tube 2 opened in the resting condition, and the grid of tube 1 which is blocked; we replace it by a common cathode resistance. Fig. 4.35 shows the circuit produced in this way.

Triggering takes place at the grid of the blocked tube 1 through a positive pulse. The falling anode voltage v_{a1} then blocks tube 2 until the coupling capacitor K has discharged sufficiently for the control effect of tube 2 to start again, causing the circuit to trigger back to the rest condition. The advantage of this circuit is obvious: The triggering process is not affected to any great extent either by the internal resistance of the release source or the associated load at the output.

Fig. 4.36 shows the course of the voltage at the anodes, the grids and the

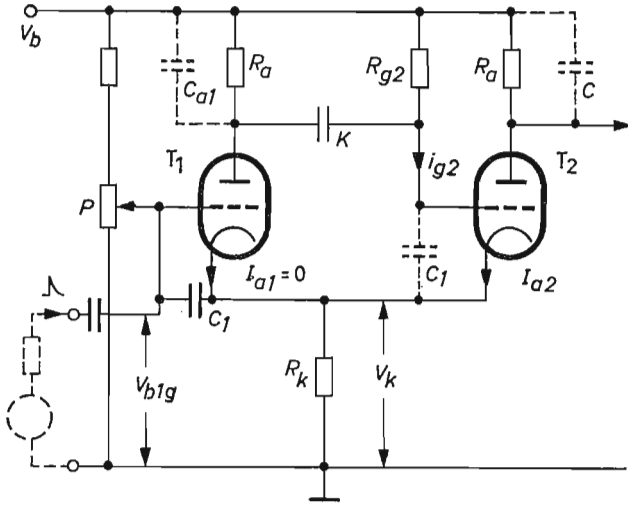


Fig. 4.35 Cathode-coupled monostable multivibrator (rest condition)

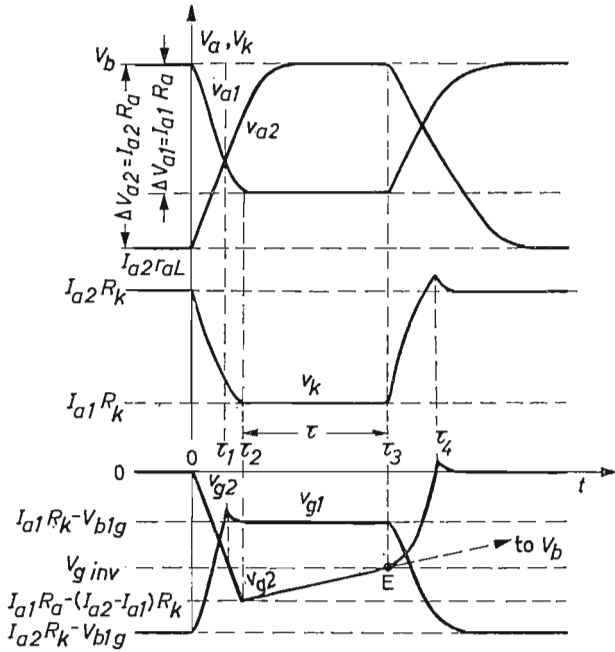


Fig. 4.36 Waveform of grid, anode and cathode voltages with a cathode-coupled monostable multivibrator

cathodes when the circuit is triggered over from the rest condition by a short positive pulse at tube 1 which raises its grid voltage above the blocking voltage. In the rest condition the cathode voltage is

$$V_k = I_{a2}R_k \quad (4.32)$$

and at the grid of tube 1 there is the voltage

$$V_{g1} = I_{a2}R_k - V_{b1g} > V_{g \text{ inv}} \quad (4.33)$$

which must be greater than the blocking voltage of tube 1. The increase of i_{a1} must be less than the decrease of i_{a2} so that the triggering process continues after the application of the trigger pulse. Then the cathode voltage decreases further, in spite of the rising anode current of tube 1, so that i_{a1} can again increase. This process is ended at period τ_1 if the grid voltage of tube 2 has exceeded the blocking voltage. Now the anode voltage v_{a1} drops further with the time constant

$$T_{ab1} = \frac{R_a r_{aL}}{R_a + r_{aL}} C_{a1} \quad (4.34)$$

to its end value $I_{a1}r_{aL}$ (moment τ_2). In all, the grid voltage of tube 2 thus undergoes the voltage jump ΔV_{a1} , diminished by the decrease of the cathode voltage jump $(I_{a2} - I_{a1})R_k$:

$$V_{gY2} = I_{a1}R_a - (I_{a2} - I_{a1})R_k \quad (4.35)$$

Now the capacitor K begins to discharge; the voltage v_{g2} exceeds the blocking voltage at moment τ_3 ; the voltage drop at R_k becomes greater until tube 1 is again blocked.

For the rest time in the quasi-stationary condition we obtain approximately

$$\tau \approx R_{g2}K \frac{I_{a1}(R_a + R_k) - I_{a2}R_k - V_{g \text{ inv}}}{V_b + I_{a1}R_a - I_{a2}R_k} \quad (4.36)$$

It can easily be demonstrated that τ is approximately linearly proportional to the bias V_{b1g} , so that we can conveniently regulate the pulse duration with the potentiometer P . The limits of the control range for V_{b1g} are given, firstly, through Equation (4.33), and secondly,

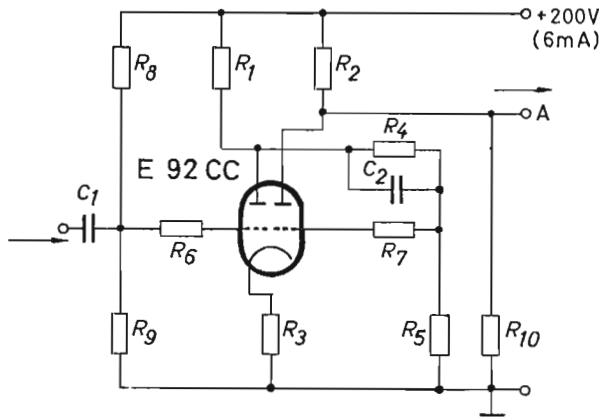
$$I_{a1}R_k - V_{b1g} < V_{g \text{ inv}}$$

must apply, according to Fig. 4.36, because of the proviso for the quasi-stationary condition of tube 1, and we thus have the condition

$$I_{a1}R_k - V_{g \text{ inv}} < V_{b1g} < I_{a2}R_k - V_{g \text{ inv}} \quad (4.37)$$

With the relations quoted here, the circuit can be calculated, as with the circuits dealt with up to now, from the size of the given output pulse, its flank steepness and duration.

If we use pulses of reversed polarity, the circuit shown in Fig. 4.35 must be transformed so that in the rest condition tube 1 conducts and tube 2 is blocked. This can be achieved through suitable bias at both grids as is shown in the circuit example of Fig. 4.37. The grid voltage of the left-hand system is kept at about zero through the voltage divider R_8/R_9 and the grid current, while the right-hand system is blocked by the voltage divider $R_5/(R_1 + R_4 + R_5)$ and the cathode voltage.



$R_1 = 5,6 \text{ k}\Omega \pm 2\%$	1 W	$R_7 = 1 \text{ k}\Omega \pm 10\%$	$\frac{1}{4}$ W
$R_2 = 5,6 \text{ k}\Omega \pm 2\%$	1 W	$R_8 = 1 \text{ M}\Omega \pm 2\%$	$\frac{1}{8}$ W
$R_3 = 5,6 \text{ k}\Omega \pm 2\%$	1 W	$R_9 = 0,39 \text{ M}\Omega \pm 2\%$	$\frac{1}{8}$ W
$R_4 = 39 \text{ k}\Omega \pm 2\%$	$\frac{1}{2}$ W	$R_{10} = 5,6 \text{ k}\Omega \pm 10\%$	1 W
$R_5 = 15 \text{ k}\Omega \pm 2\%$	$\frac{1}{4}$ W	$C_1 = 0,47 \text{ }\mu\text{F}$	
$R_6 = 1 \text{ k}\Omega \pm 10\%$	$\frac{1}{4}$ W	$C_2 = 15 \text{ pF}$	

Fig. 4.37 Circuit of a cathode-coupled monostable multivibrator

While positive input pulses over C_1 do not change the condition of the circuit (limiting through resistance R_6), it is released by a negative pulse of about 20 V amplitude and at least $1 \mu\text{s}$ duration. At the anode of the right-hand system we then have a negative pulse whose duration is determined through the rest time in the quasi-stationary condition produced by the recharging of C_2 . This circuit can be used as a pulse former for transforming input pulses taken at random within certain limits, into defined pulses such as is necessary, for instance, in counter circuits.

4.2.2 BISTABLE FLIP-FLOP CIRCUIT WITH TRIGGER TUBES

Although a trigger tube is a bistable element in itself, (extinguished and ignited conditions), in some cases bistable circuits are required which permit simultaneous use of both stationary conditions. This is possible with appropriate coupling of two trigger tubes whereby, as with the multivibrator, the extinguished condition of one tube governs the ignited condition of the other, and vice versa. Fig. 4.38 shows this kind of circuit. It is based on the fact that the voltage drop at the cathode resistance produced when one tube is ignited, extinguishes the conducting tube. At first, tube 1 must be ignited: Then the voltage

$$V_{k1} = V_b - V_{arc} = I_a R \quad (4.38)$$

is present at the cathode of the first tube and thus also, via R_T at the trigger of tube 2. This voltage must be so low that tube 2 is not yet lit, and yet it must be high enough for this tube to be ignited by the next trigger pulse.

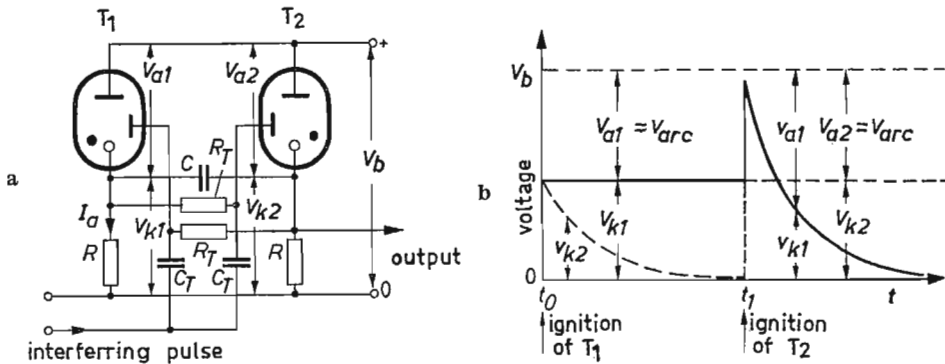


Fig. 4.38 A bistable flip-flop circuit with two trigger tubes

At the moment of ignition of tube 2, the voltage at its cathode resistance jumps to the value $V_{k2} = V_b - V_{arc}$. This voltage jump adds itself to the voltage at the coupling capacitor C , so that the voltage v_{k1} lies momentarily at the cathode of tube 1 and the burning voltage is below the required value and tube 1 is thus extinguished.

Now v_{k1} drops to zero with the time constant

$$\tau = RC \quad (4.39)$$

This voltage waveform is shown in Fig. 4.38 b. The voltage v_{a1} at the extinguished tube must not rise too quickly, to prevent fresh ignition of the

tube (see Section 3.2.2). The maximum switching frequency of this flip-flop circuit is limited in this way.

The following can be stated concerning the choice of circuit component values: The cathode resistance R is chosen so that with the constant current I_a , selected or available, the cathode voltage is still safely below the ignition voltage. The necessary feed voltage V_b is then obtained from Equation (4.38). To achieve a high switching frequency, capacitor C must be chosen just small enough that the extinguished tube is not re-ignited.

Because of the coupling capacitor C_T , the trigger voltage does not directly follow the cathode voltage so that a limiting of the maximum switching frequency can also arise here. Too small values of C_T and R_T , on the other hand, lead to distortion of the output pulse. In practice we take approximately

$$R_T C_T \approx R C$$

The following values are obtained for a circuit with tube Z 70 U:

$$\begin{array}{ll} R = 80 \text{ k}\Omega & R_T = 1 \text{ M}\Omega \\ C = 3.3 \text{ nF} & C_T = 330 \text{ pF} \end{array}$$

in which the maximum switching frequency amounts to about 3 kc/s and the required release amplitude is about +80 V.

4.2.3 TRANSISTOR CIRCUITS

Bistable and monostable circuits consisting of transistors (in emitter circuits) are superficially very little different from the corresponding tube circuits. When considering the component values in the circuit and its efficiency, however, there are a number of special features due to the characteristic properties of transistors. While the switching speed is limited in tube circuits by harmful parallel capacitances, limits are set here as a result of the necessary charging time and the load storing in the base space (see Section 3.4.2). In addition, the low input resistance of the opened transistor must be borne in mind when the voltage and current distribution in the circuit is calculated, as we usually base the assessment of a circuit on the current. Finally, with a transistor, the feed voltage is lower by about 1 to 2 orders, which means a correspondingly smaller output pulse, though the ratio of output voltage to feed voltage is in general considerably higher than with tubes. As long as we work with pure transistor circuits, the low value of the output pulse is no drawback. A further peculiarity of transistor circuits is that the switching speed depends on the magnitude of the control and thus also on the stability

of the switching positions. Great stability calls for adequate over-control of the collector which, in turn, impairs the switching time. The switching speed can only be raised as far as is compatible with working security.

Calculation of the circuit usually proceeds from a known output voltage and switching time. The output voltage is limited through the considerations discussed in Section 3.4.3, while the switching time generally depends on the limiting frequency of the type of transistor used. (see Section 3.4.2) Finally, with frequent switching, it is necessary to ensure that the permissible leakage capacitance of the transistor is not exceeded by the effective leakage capacitance. The value of the collector current of the blocked transistor plays an important part in the thermal stability of the circuit.

Certain difficulties can occur if a bistable multivibrator constructed with transistors is used in combination with further multivibrators or other transistor circuits. On one hand, the output of the circuit cannot be loaded too much, and on the other, the input for the release pulse is usually low resistance so that the direct coupling of two stages can produce difficulties. Furthermore the coupling capacitors have an unfavourable effect on the switching time. These disadvantages can be avoided to a great extent by an asymmetrically constructed circuit [52]. This, however, is susceptible to spreads in the transistors and resistances as well as to supply voltage fluctuations.

4.2.3.1 Bistable multivibrator [52]

Fig. 4.39 shows a circuit for a symmetrically constructed bistable multi-

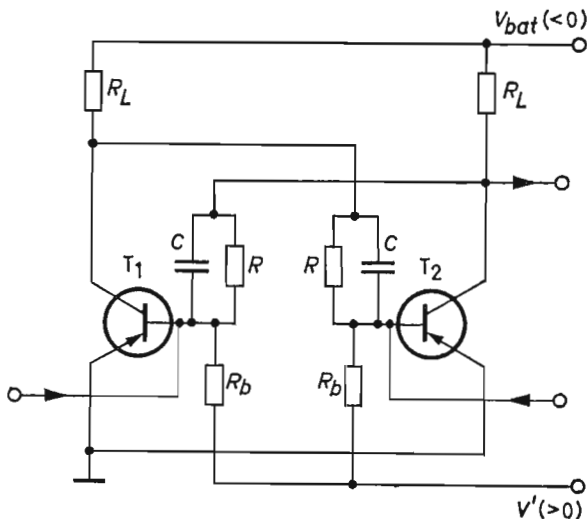


Fig. 4.39 Symmetrical bistable multivibrator

vibrator analogous to the circuit in Fig. 4.22. Let us assume that transistor T_2 is conducting, for example, and T_1 is blocked. A positive pulse at the base of T_2 then blocks this transistor whose collector current in turn opens T_1 . The rising collector voltage of T_1 proceeds via the coupling capacitor C at the base of T_2 in the same way as the applied release pulse; and the circuit switches over into the other stable position.

The choice of resistances R and R_b depends upon the stable conditions of the circuit. The control of the transistors in opened and blocked conditions established in this way, together with the coupling capacitor C , however, also influence the transit behaviour of the circuit, its output sensitivity and stability against interference, particularly from temperature fluctuations.

Static design:

In the two stable conditions, one transistor is blocked at one time, the other opened. The voltage divider from the collector to the base must therefore fulfil two conditions: It must first keep the base of one transistor positive when the other is opened, that is for all values of the base residual current I_{BY} (which is strongly dependent on temperature; see Section 3.4.1); and secondly, it must open one transistor with sufficient certainty (for the least occurring current amplification), when the other is blocked.

Fig. 4.40a shows the voltages and currents when T_1 is blocked and T_2 is opened. For the base voltage of T_1 in the blocked condition we then obtain

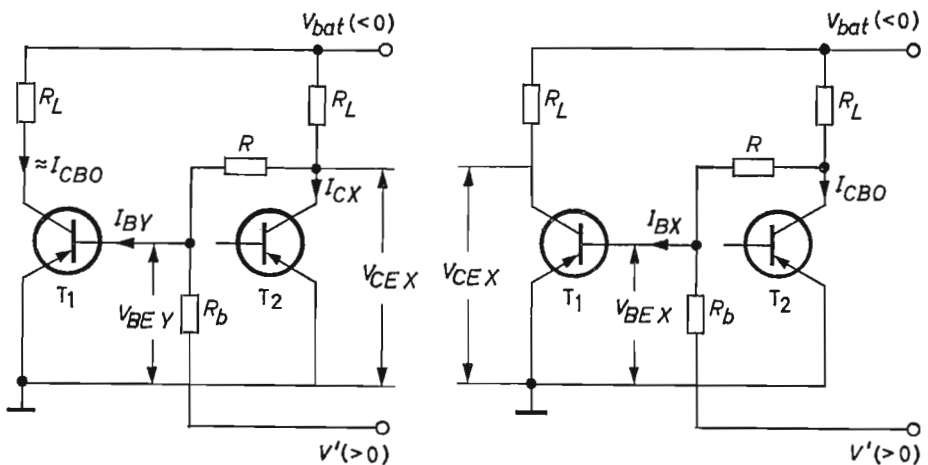


Fig. 4.40 The stable conditions

$$V_{BEY} = V_{CEX} + \frac{R}{R + R_b} (V' - V_{CEX}) - \frac{R R_b}{R + R_b} I_{BY} \quad (4.40)$$

Provided V_{BEY} is sufficiently positive, we can substitute the collector residual current $-I_{CB0}$ for the base residual current I_{BY} (see Fig. 3.14). The resistors R and R_b must now be chosen so that V_{BEY} blocks transistor T_1 adequately. For R_b then the condition

$$R_b < R \frac{V' - V_{BEY}}{V_{BEY} - V_{CEX} - RI_{CB0}} \quad (4.41)$$

(follows from Equation (4.40).

This relation must be fulfilled even with the most unfavourable working conditions; we therefore give to I_{CB0} the maximum possible value which can be set at the upper temperature limit of the circuit.

Fig. 4.40b shows the currents and voltages in the other stable condition when T_1 is opened and T_2 is blocked. The base voltage for T_1 is then

$$V_{BEX} = V_{bat} + \frac{R_L + R}{R_L + R + R_b} (V' - V_{bat}) - I_{BX} \frac{R_b (R_L + R)}{R_L + R + R_b} \quad (4.42)$$

Here the voltage divider current in the collector resistance

$$i = \frac{V' - V_{CEX}}{R + R_b}$$

has been disregarded. In order to keep the error implied in Equation (4.42) to less than 5%, it is necessary for

$$i \leq 0.05 I_{CX}$$

and for the sum of the voltage divider resistances we obtain the condition

$$R + R_b \geq \left| \frac{R_L (V' - V_{CEX})}{0.05 (V_{bat} - V_{CEX})} \right| \quad (4.43)$$

So that the voltage V_{BEX} opens T_1 , it must be equal to or more negative than the base voltage required for the initial base current I_{BX} (see Equation (3.10)), and from Equation (4.42), we obtain the relation

$$R_b > R \frac{V_{BEX} - V'}{V_{bat} - V_{BEX} - \frac{V_{bat} - V_{CEX}}{1 + R_L/R} - \frac{V_{bat} - V_{CEX}}{\alpha_e R_L/R}} \quad (4.44)$$

in which we have replaced the base current I_{BX} by the relation

$$I_{BX} = \frac{I_{CX}}{\alpha_e} \approx \frac{V_{bat} - V_{CEX}}{\alpha_e R_L}$$

The smallest possible value must be given to $\bar{\alpha}_e$ (most unfavourable transistor, lowest ambient temperature).

With a given type of transistor, prescribed collector resistance and feed voltage, the required voltage divider can be calculated from Equations (4.41), (4.42) and (4.43). This can most easily be carried out graphically if the three curves for R_b are drawn as functions of R . The solution should then lie within the area circumscribed by the three curves. If no such area is plotted, circuit design is impossible under the conditions mentioned [90].

Dynamic behaviour:

The charging of the base layer necessary to open a transistor can be compensated by an appropriately large input capacitance (see Section 3.4.2). For this reason, a comparatively big coupling capacitor C is needed to avoid a strong voltage division, though this again increases the switch-off time. The most favourable value is obtained for C when the switch-on and off times are about equal in amount.

By rule of thumb methods, C can be calculated from the relation

$$R_L C \geq 1/f_{ab} \quad (4.45)$$

where f_{fall} is the limiting frequency of the transistor in the base circuit. If transistor T_2 in Fig. 4.39 is opened and T_1 blocked, the multivibrator is now switched over through a positive pulse at the base of T_2 . During the storing time τ this pulse first discharges the excess load from the base space (compare Fig. 3.15). With further discharging, the collector current of transistor T_2 drops within time t_c , which corresponds approximately to time t according to Equation (3.17), to the residual current. The voltage rises to $V_{CEY} \approx V_{bat}$ as is shown in Fig. 4.41. A charging current thus flows via R_L and C into transistor T_1 and opens it.

The collector voltage V_{CE1} is then reduced to the residual voltage ($V_{CE0} = V_{CEX}$). In this way, the base voltage becomes strongly positive via C . In time t_b , V_{BE2} drops to the stationary value V_{BEY} . Time t_b thus determines the recovery time of the circuit. Nevertheless, the circuit can already be switched over again within interval t_b ; then, however, the charging pulse

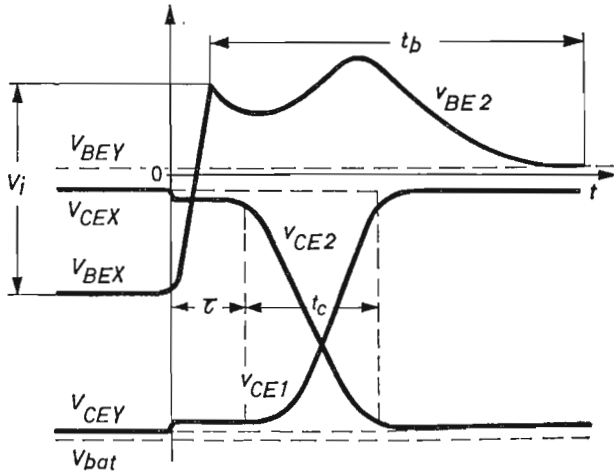


Fig. 4.41 Collector and base voltages at the blocking of T_2 and opening of T_1 through a positive pulse of amplitude V_i at the base of T_2

from the collector of transistor T_1 must not only build up the load in the base space of T_2 but must also break down the residual load of the capacitor C .

Sensitivity

The sensitivity depends to a great extent on the stability of the circuit, which can be influenced by the choice of the resistances R and R_m .

The greatest sensitivity is achieved with the maximum possible values of R . Then, however, the circuit would be very susceptible to interfering pulses and to spreads in the components, so that experience shows that it is best to keep to the middle of the range given on the basis of the two stable positions (see Equations (4.41), (4.43) and (4.44).

The required input pulses are usually of equal value to the output pulses. This offers the advantage that one stage can directly drive the following one. The trigger pulses are generally allowed to operate at the base. With multi-vibrators which have to be triggered back and forwards over a single line, the coupling is best done through diodes so that the input pulse can only influence the transistor open at the time. The coupling capacitor C_i is chosen about equal to capacitor C . Fig. 4.42 shows the fundamental arrangement. Here the negative bias V_D is chosen so that

$$|V_{BEX}| > |V_D| > |V_{BEY}|$$

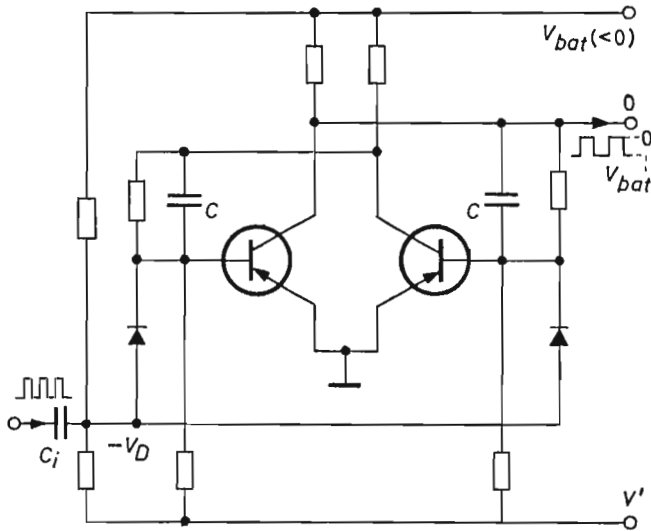


Fig. 4.42 Coupling of the release pulses via diodes

The positive pulse then only operates at the transistor open at the time.

For reliable operation, the circuit makes several demands on the constancy of the supply voltages. In the following examples a circuit will first be described which is less critical in operation.

Circuit examples:

Fig. 4.43 shows a practical circuit. The triggering of the multivibrator takes place at a common line through the diodes D ; these are so biased via the resistances R_T , through the collector voltages, that a pulse is only transmitted at the opened transistor and then only in a positive direction. The input pulses are differentiated by suitable dimensioning of C_T and R_T so that the rear flank of the multivibrator reverses if negative square-wave pulses are used for release. The circuit is constructed with transistors OC 71 and OC 46. Table 4.1 gives the dimensions.

TABLE 4.1: CIRCUIT COMPONENT VALUES IN FIG. 4.43

T_1 and T_2	R k Ω	R_b k Ω	R_c k Ω	R_T k Ω	C pF	C_T pF
OC 71	15	47	3.3	8.2	1000	2000
OC 46	12	50	3.3	8.2	200	300

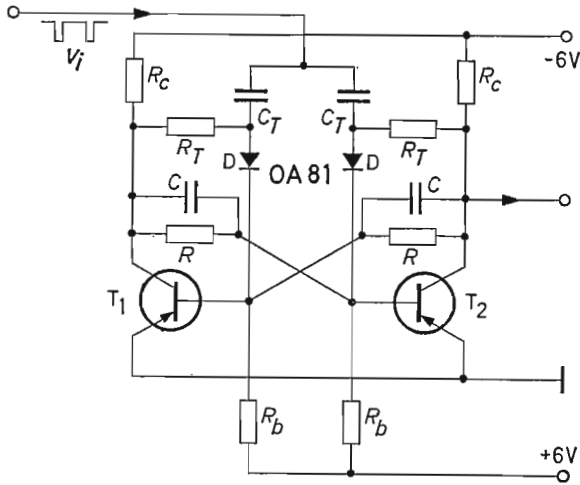


Fig. 4.43 Bistable multivibrator with the transistors OC 71 and OC 46

The permissible spreads amount to $\pm 5\%$ for the resistances and $\pm 10\%$ for the capacitors; the feed voltage can fluctuate by $\pm 10\%$. Table 4.2 shows the working data for the circuit. The permissible collector load for the switched-on transistor may amount to a minimum of $2.7 \text{ k}\Omega$ at -6 V , for the blocked transistor about $40 \text{ k}\Omega$ at $+6 \text{ V}$ and $15 \text{ k}\Omega$ at 0 V .

TABLE 4.2: WORKING DATA OF CIRCUIT IN FIG. 4.43

Transistor	Input pulse		Max. ambient temperature $^{\circ}\text{C}$	Max. switch frequency kc/s
	V	μs		
OC 71	+ 4	≥ 2	+ 45	35
	- 4	≥ 20		
OC 46	+ 4	≥ 0.4	+ 45	180
	- 4	≥ 2.0		

Fig. 4.44 shows a further example in which the base bias is generated across the bypassed emitter resistance R_e . The circuit was built up with the transistors OC 71 and OC 46. The necessary coupling capacitor C , the trigger voltage and the measured switching times are given in Table 4.3. Fig. 4.45 shows the dependence of the necessary trigger pulse V_i or I_i on the voltage divider resistance R and the capacitor C .

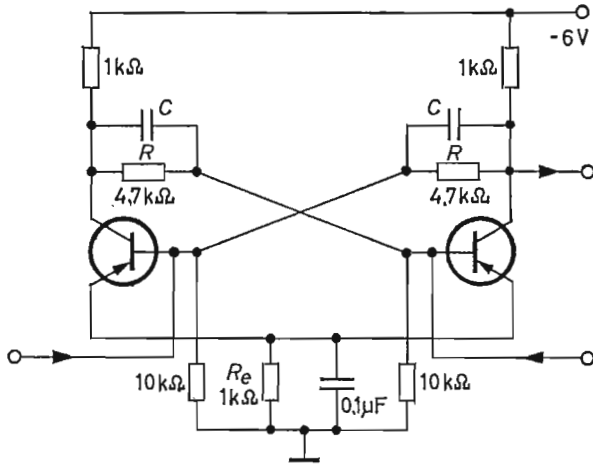


Fig. 4.44 Circuit with transistors OC 71 and OC 46

TABLE 4.3: SUPPLEMENTARY DATA FOR CIRCUIT IN FIG. 4.44

Transistor	OC 71	OC 46
Coupling capacitor C	1000 pF	100 pF
Trigger pulse	1 V	1 V
Switching time	5 μs	0.6 μs

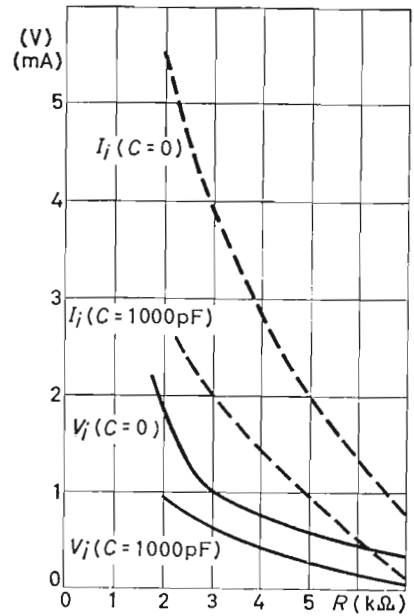


Fig. 4.45
Dependence of the release sensitivity on resistance R and capacitor C in Fig. 4.44

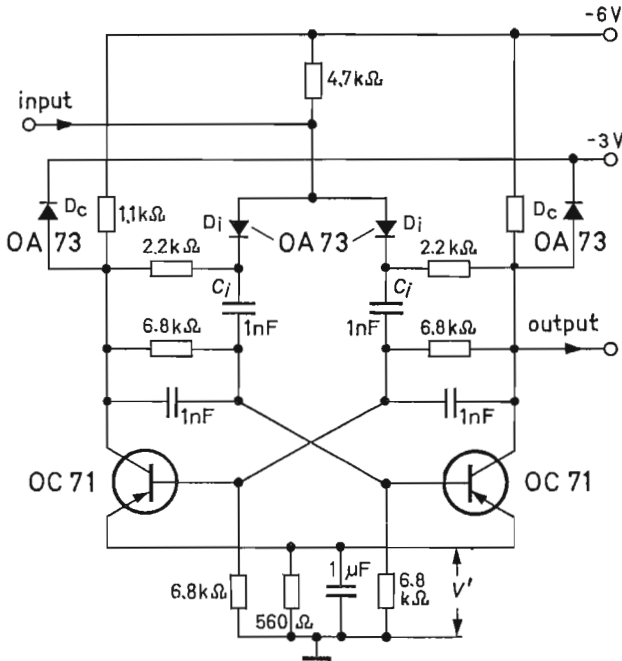


Fig. 4.46 Circuit with diode control limiting and diode coupling of the release pulses

As a further example, Fig. 4.46 shows the circuit of a bistable multivibrator [53] in which the collectors are kept at a lower voltage than the feed voltage through the diodes D_c . These diodes keep the collector of the opened transistor at -3 V. The maximum switching speed and the release sensitivity are therefore raised. The coupling of the release pulse also takes place via diodes D_i whose bias is controlled by the collectors. These diodes are so biased that positive release pulses alone can operate and then only (via C_j) at the base of the opened transistor, since this diode alone is suitably biased through the high negative collector voltage of the other transistor. The multivibrator works up to a switching frequency of 100 kc/s; a release pulse of 1 V is needed up to about 20 kc/s and of 3 V above that.

4.2.3.2 Monostable multivibrator [52]

Complying to the tube circuit (Fig. 4.33) we here also obtain the monostable from the bistable circuit by omitting the direct coupling in a coupling section, as shown in Fig. 4.47. Transistor T_1 is opened in the rest position via R_{b1} , and T_2 is blocked by the bias V' . A positive pulse at the base of T_1 triggers

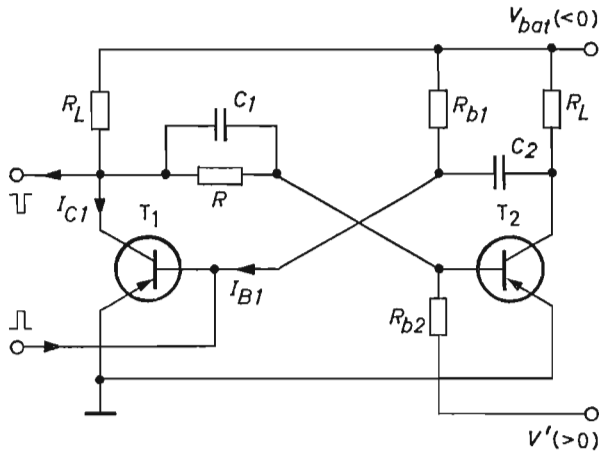


Fig. 4.47 Monostable multivibrator

the circuit over into the quasi-stable condition. The course of the voltage then produced is shown in Fig. 4.48. The release pulse at T_1 must make transistor T_2 conduct to such an extent that the feedback can commence. The quasi-stable condition is then quickly reached. As soon as the base voltage at T_1 , after time τ , reaches the voltage at which the collector current commences, the feedback is again effective; the circuit triggers back into the resting position. The resultant drop in collector voltage of T_2 causes an overswing of the base voltage V_{BE1} . The rest time, τ , of the circuit in the quasi-stable condition is largely determined by the time constant $R_{b1}C_2$. The circuit is dimensioned as far as R_{b1} and C_2 according to the relations for the bistable multivibrator. R_{b1} must be chosen large enough for transistor T_1

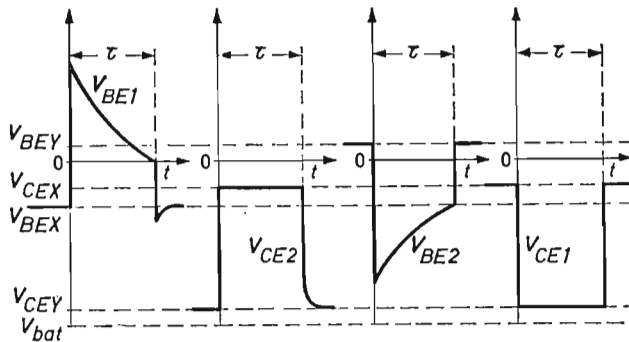


Fig. 4.48 Voltage waveform with the monostable multivibrator

to be fully controlled, though excessive control reduces the sensitivity of the circuit. Ignoring the voltage drop at the base line resistance and at the emitter diode,

$$\left| \frac{V_{bat}}{R_{b1}} \right| \approx |I_{B1}| > \left| \frac{I_{C1X}}{\alpha_{e\ min}} \right| \approx \left| \frac{V_{bat}}{R_L \alpha_{\ min}} \right|$$

or

$$R_{b1} < R_L \bar{\alpha}_{\ min}$$

when $\bar{\alpha}_{\ min}$ is the lowest value of the static current amplification of the opened transistor T_1 . The resistance R_{b1} is thus established through R_L and the transistor, so that the rest time τ of the circuit can only be set through C_2 . We find

$$\tau = R_{b1} C_2 \ln \frac{2 V_{bat} + I_{CB0} (R_{b1} - R_L) - V_{BE1X} - V_{CE2X}}{V_{bat} + I_{CB0} R_{b1}} \quad (4.47)$$

in which V_{BE1X} is the base voltage of the opened transistor T_1 (see Equation (3.10)) and V_{CE2X} is the residual voltage of transistor T_2 . The items with I_{CB0} , V_{BE1X} and V_{CE2X} are small, as a rule, and can usually be ignored so that for τ we have the approximation

$$\tau \approx 0.7 R_{b1} C_2 \quad (4.48)$$

To minimise the influence of the temperature-dependent residual current, I_{CB0} , $-I_{CB0} R_{b1}$ and $-I_{CB0}(R_{b1}-R_L)$ must be small in comparison with $-V_{bat}$, as follows from Equation (4.47). We find from experience that the rest time does not work out less than

$$\tau \approx 10/f_{ab} \quad (4.49)$$

where f_{fall} is the limiting frequency of the base circuit.

To prevent input and output lying in the feedback section, we can use the circuit shown in Fig. 4.49 with emitter coupling. This is similar to the cathode-coupled tube circuit (see Fig. 4.35). At the same time we thus ensure through diode D that T_2 keeps a constant base voltage in the blocked condition which raises the constancy of the rest time τ . In the rest position transistor T_1 is conducting as a result of the base current over R_{b1} . At resistance R_e the emitter current of T_1 then produces a negative voltage drop and diode D is opened. Its voltage drop (some 0.1 V) thus serves as blocking voltage for transistor T_2 .

A negative release pulse brings the circuit into the quasi-stable position by which the pulse across C_i is differentiated. In this way the collector current at T_1 becomes more negative and opens transistor T_2 .

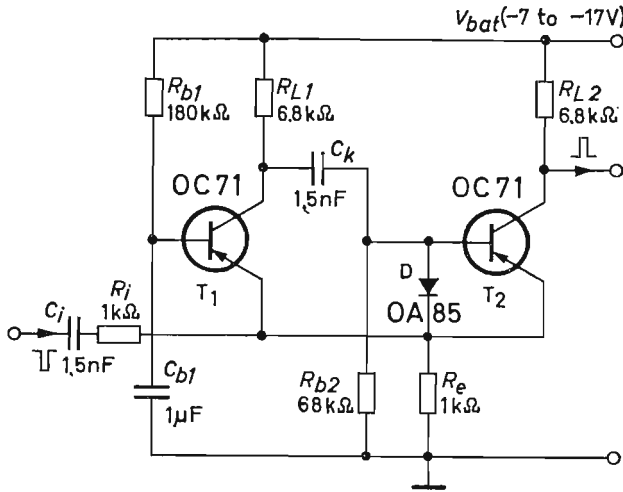


Fig. 4.49 Emitter-coupled monostable multivibrator

This process occurs rapidly because of the feedback over C_k and the common emitter resistance. During the quasi-stable condition T_2 is controlled and T_1 blocked because the additional recharging current of capacitor C_k brings about a greater voltage drop at the emitter resistance R_e than in the stable condition. If the base-emitter voltage of T_2 becomes zero during the discharge of C_k over R_{b2} , the circuit triggers back again. The output pulse produced at the collector of T_2 has the form shown in Fig. 4.50. Between a and b, transistor T_2 begins to conduct through the influence of the trigger pulse (across T_1). At point b the total amplification of the circuit rises above 1 and the feedback determines further progress. Between c and d, T_2 is controlled; between d and e, the charging current of C_k is no longer sufficient to keep T_2 open and the collector current I_{C2} drops. From point e the circuit finally triggers back again.

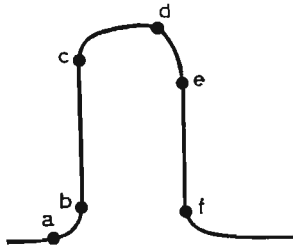


Fig. 4.50 Output pulse of the circuit in Fig. 4.49

With a fluctuation of the supply voltage between -7 and -17 V, the required release amplitude lies between 0.4 and 0.7 V. The duration of the output pulse then varies between about 32 and 36 μs . The circuit, however, has a number of drawbacks. Its properties depend considerably on the spreads of the type of transistor used. With a low $\bar{\alpha}_e$ of T_1 , the circuit begins to oscillate. On the other hand, the current amplification of transistor T_2 enters essentially into the rest time (with an $\bar{\alpha}_e$ variation of 16 to 110 , τ oscillates between 30 and 68 μs). These influences have the following causes: The base current of T_1 is mainly determined by R_{b1} , i.e. if T_1 has great current amplification, it is more controlled and the pulse duration is thus prolonged (because of the storage effect). On the other hand, a small $\bar{\alpha}_e$ of T_1 is not enough to block T_2 , which causes instability. The effect of T_2 on the pulse duration lies above all in the fact that with a high $\bar{\alpha}_e$ a small base current is sufficient to control the transistor fully, i.e. the discharge of the coupling capacitor C_k keeps transistor T_2 open longer than with a small $\bar{\alpha}_e$. Fig. 4.51 shows a circuit (with about 50 μs pulse duration) which, to a great extent, avoids the disadvantages of the circuit in Fig. 4.49. The diode D is now biased (1 to 1.5 V) so that T_2 is blocked adequately with a small $\bar{\alpha}_e$. Because of the counter-coupling between collector and base of transistor T_2 through the

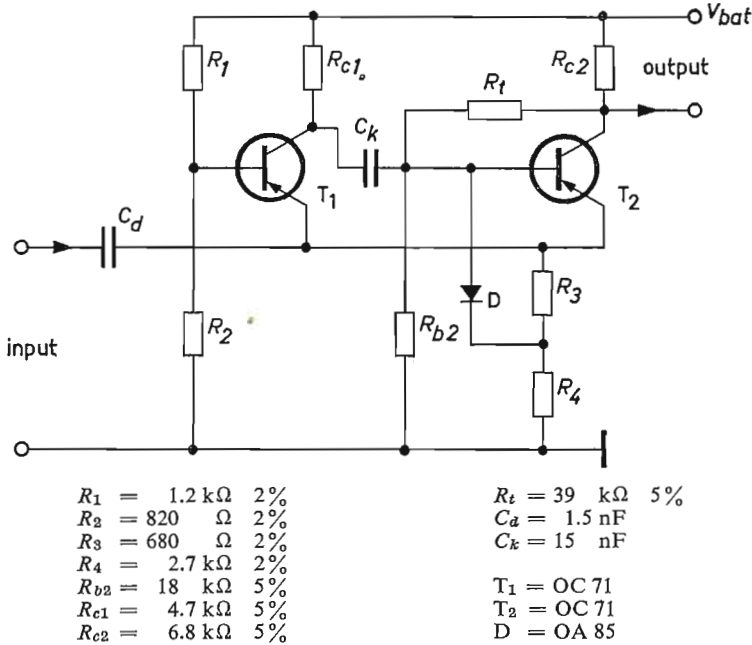


Fig. 4.51 Improved circuit derived from Fig. 4.49

resistance R_b , the influence of its current amplification is reduced. Through generation of the base voltage for T_1 across a voltage divider, we finally achieve the situation whereby the opening current of transistor T_1 is in inverse proportion to $\bar{\alpha}_e$.

The circuit in Fig. 4.51 is practically independent of the ambient temperature up to about 50 °C. The deviation of the pulse duration influenced by spreads of transistors amounts to about $\pm 10\%$ of the mean value, while a change of the feed voltage between 7 and 17 V affects the pulse duration by about $\pm 3\%$.

4.3 Decade counters

The decade counter (see Sections 2.4.3 and 2.6.2) is the main component for computing in the decade system (see Section 2.8.4). We recognise in it a circuit which can take in ten different stable conditions passed in fixed sequence, when ten pulses are conveyed to the input. The tenth pulse brings the counter back to the zero position whereby a pulse is simultaneously delivered to the output. Decade counters of this type can be constructed with vacuum tubes, gasfilled tubes, transistors and rectangular ferrite cores.

4.3.1 COUNTER CIRCUITS WITH TRIODES

Counter circuits with tubes are rapid in operation and so their demands for space and extra switching equipment as well as their energy consumption are relatively large.

We shall first describe a decade counter with 150 kc/s maximum counting frequency, constructed with the tube E 92 CC. Its bistable multivibrators comply with the statements in Section 4.2.1.1 and are only switched through negative pulses. The first three stages are connected together in the usual way (Fig. 2.10). As Fig. 4.52 shows, the fourth stage, M_3 , however, is only coupled

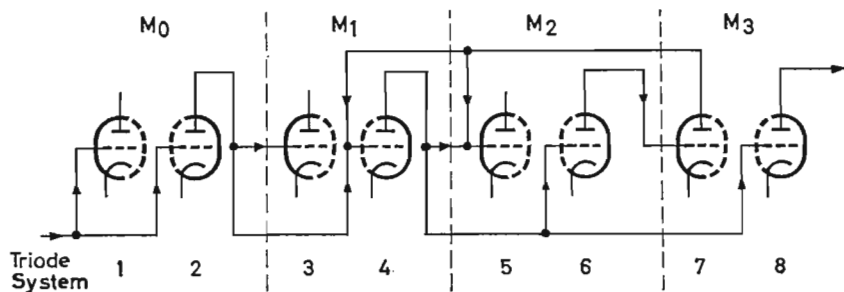


Fig. 4.52 Coupling of the four stages of a decade counter with the weights 1-2-4-2

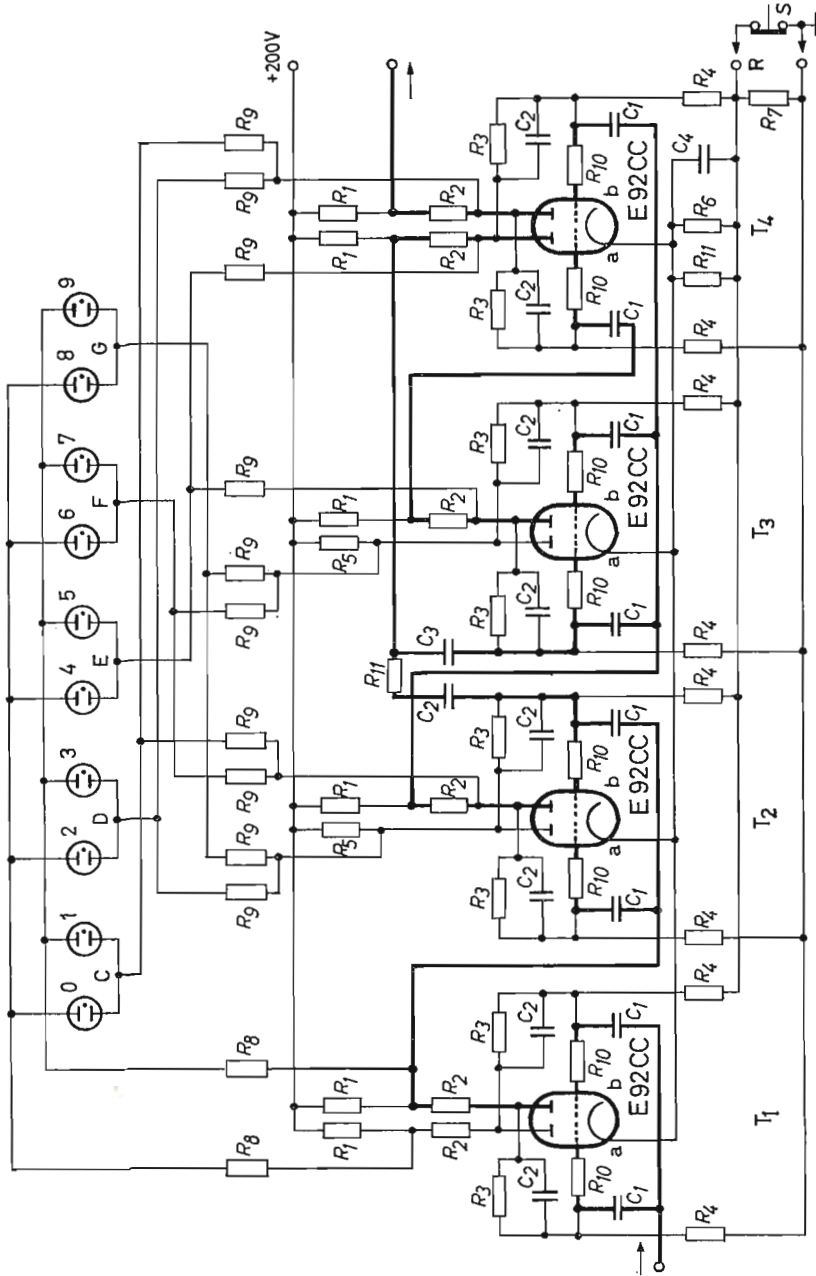


Fig. 4.53 Decade counter with E 92 CC (for dimensions see Table 4.5)

TABLE 4.5: COMPONENT VALUES FOR CIRCUIT IN FIG. 4.53

$R_1 = 12$	$k\Omega$	1 W	2%	$R_9 = 0.47$	$M\Omega$	$1/4$ W	5%
$R_2 = 15$	$k\Omega$	1 W	2%	$R_{10} = 1$	$k\Omega$	$1/2$ W	10%
$R_3 = 68$	$k\Omega$	1 W	2%	$R_{11} = 22$	$k\Omega$	$1/2$ W	10%
$R_5 = 27$	$k\Omega$	$1/4$ W	2%	$C_1 = 33$	pF		5%
$R_4 = 22$	$k\Omega$	2 W	2%	$C_2 = 100$	pF		5%
$R_7 = 1$	$k\Omega$	2 W	2%	$C_3 = 68$	pF		5%
$R_6 = 2.2$	$k\Omega$	$1/2$ W	10%	$C_4 = 0.01$	μF		10%
$R_8 = 0.22$	$M\Omega$	$1/4$ W	5%				

The neon lamps are connected to the anodes of the individual systems so that the one whose value corresponds to the number of pulses fed in lights up.

Fig. 4.54 shows another circuit of a decade counter. This one, using the double triode E 88 CC has a limiting frequency of 5 Mc/s. The high counting frequency requires several extra measures: The coupling of the counter pulse at the grid occurs via fast operating diodes with high blocking resistances (OA 81); the grid voltage jumps are limited by diodes (so that here only the initially rapid rise of the grid voltages is effective); and in conclusion, the harmful parallel capacitances at the anodes are partly compensated in the two first stages through series inductances. The feedback corresponds to Fig. 4.52. The negative input pulses must be about 10 V and the rise time about $0.05 \mu s$. With the jump into zero position, the counter yields a negative output pulse of about 17 V and $0.3 \mu s$ rise time. The load capacitance at the output may amount to as much as 20 pF.

On account of the low anode voltage jump, we rely on indicator tubes here for an indication of the counter position. The DM 160 tubes used here fall successively into the units 1, 2, 4 and 2 in accordance with Table 4.4. The counter can be quickly brought to zero position at any time by manual operation of key S. In this way, all the cathodes of the left-hand system are separated from the cathode resistance and are thus blocked.

4.3.2 RING COUNTERS WITH THE TRIGGER TUBE Z 70 U

For counting circuits with a maximum counting frequency below 3 kc/s, ring counters can be very simply constructed with trigger tubes (see Section 3.2). The chief advantages here are that each bistable element only needs one tube and that its glow can serve as an indicator of the condition. Since in most ring counters only one system carries current at a time, the energy consumption and thus the heating are very low. In conclusion, the small size of cold cathode tubes is very convenient for modern construction methods. Relatively high feed voltages (200 to 300 V) and release pulses (60 to 100 V) are however, necessary.

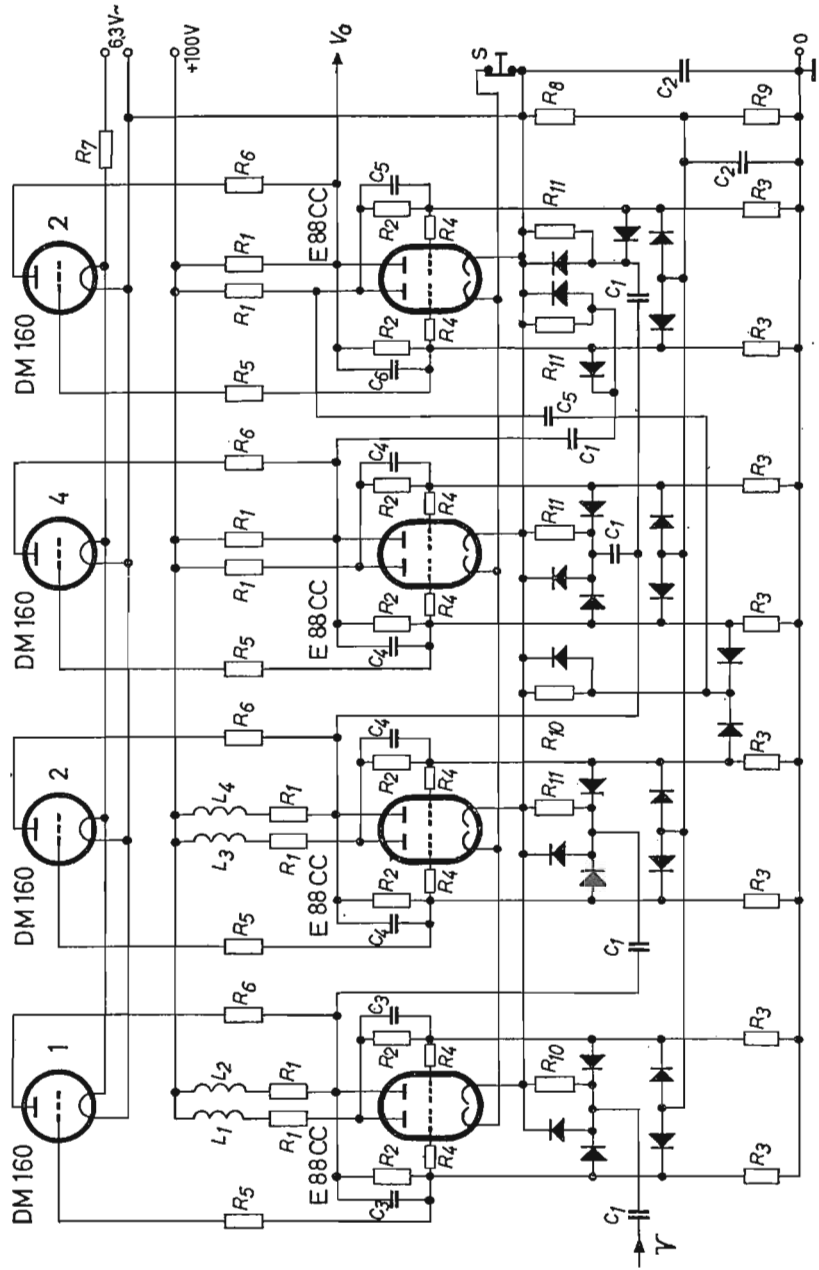


Fig. 4.54 Decade counter with E 88 CC (for dimensions see Table 4.6)

TABLE 4.6: COMPONENT VALUES FOR CIRCUIT IN FIG. 4.54

$R_1 = 1.5 \text{ k}\Omega$	$\frac{1}{2} \text{ W}$	2%	$L_1 = 30 \text{ }\mu\text{H}$
$R_2 = 22 \text{ k}\Omega$	$\frac{1}{4} \text{ W}$	1%	$L_2 = 50 \text{ }\mu\text{H}$
$R_3 = 15 \text{ k}\Omega$	$\frac{1}{4} \text{ W}$	1%	$L_3 = 100 \text{ }\mu\text{H}$
$R_4 = 220 \text{ }\Omega$	$\frac{1}{2} \text{ W}$	10%	$L_4 = 80 \text{ }\mu\text{H}$
$R_5 = 1 \text{ M}\Omega$	$\frac{1}{8} \text{ W}$	10%	$C_1 = 22 \text{ pF}$
$R_6 = 68 \text{ k}\Omega$	$\frac{1}{2} \text{ W}$	10%	$C_2 = 10 \text{ nF}$
$R_7 = 44 \text{ }\Omega$	1 W	5%	$C_3 = 27 \text{ pF}$
$R_8 = 120 \text{ }\Omega$	$\frac{1}{2} \text{ W}$	2%	$C_4 = 47 \text{ pF}$
$R_9 = 680 \text{ }\Omega$	3 W	2%	$C_5 = 68 \text{ pF}$
$R_{10} = 1 \text{ k}\Omega$	$\frac{1}{2} \text{ W}$	10%	$C_6 = 100 \text{ pF}$
$R_{11} = 2.2 \text{ k}\Omega$	$\frac{1}{2} \text{ W}$	10%	

The two stable conditions are given by the extinguished and ignited tube. Following on the statements in Section 2.4.3.2 concerning bistable elements used in ring counters, circuits with trigger tubes must be constructed to comply with the points mentioned below: If a tube is conducting, it must be possible to ignite the succeeding tube by an input pulse. At the same time, the ignition of this tube must extinguish the previous one. The first requirement can be met by coupling the starter of each tube to the cathode resistance of the preceding one (Fig. 4.55a). Through the voltage drop at the conducting tube, the starter of the next tube is then so biased that the next counting pulse of suitable value ignites this tube while it is not sufficient to light up the remainder. On the other hand, the anode current pulse produced can be used to extinguish the previous tube, so that we either give the tubes a common anode resistance or an additional common cathode resistance, or couple their cathodes capacitively together.

Fig. 4.55a shows the coupling of two tubes in a ring counter with a common

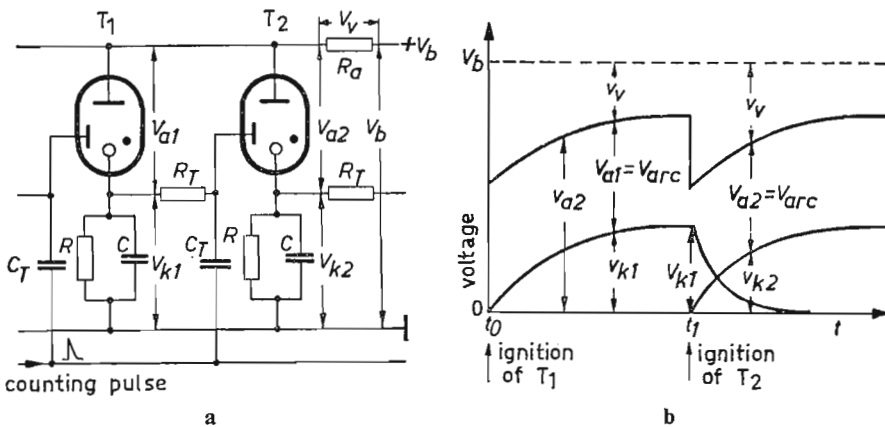


Fig. 4.55 Two elements of a ring counter with common anode resistance

anode resistance R_a . After ignition of tube 1, the cathode voltage v_{k1} rises exponentially from zero to the end value

$$V_{k1} = I_a R \quad (4.50)$$

given by the burning current I_a of the tube, namely with the time constant

$$\tau_1 = \frac{R R_a}{R + R_a} C \quad (4.51)$$

Thus, for the feed voltage we have:

$$V_b = V_{arc} + I_a (R_a + R) \quad (4.52)$$

The voltage V_{k1} must be less than the ignition voltage V_{t2} at the starter so that the ignition of the second tube only occurs through the next igniting pulse. We normally put

$$V_{k1} = \frac{V_{st} z}{\alpha} \quad (4.53)$$

where the factor of safety $\alpha > 1$. The counting pulse itself must then, with adequate safeguards, bring the voltage at the starter above the ignition voltage:

$$V_i = \beta (V_{st} z - V_{k1}) \quad (4.54)$$

where, for guaranteed ignition, β must again > 1 . Moreover, the duration of the ignition pulse must lie sufficiently above the ignition time of the tube (see Section 3.2.2).

When tube 2 is ignited, the cathode resistance is briefly short-circuited in the first instant through the capacitor C , so that here we have

$$V_b = V_{arc} + I_{a0} R_a \quad (4.55)$$

with I_{a0} as the burning current of the tube for $v_{k2} = 0$. With the help of Equations (4.50), (4.52) and (4.53), we can calculate resistances R_a and R and the required pulse amplitude V_i at a given feed voltage V_b and permissible constant current I_a . Equation (4.55) then supplies the maximum tube current I_{a0} at the moment of ignition of the tube. Immediately after ignition of tube 2, there is only the voltage

$$v_{a1} = V_{arc} - V_{k1} \quad (4.56)$$

at tube 1, so that it is extinguished. After tube 1 is extinguished its cathode voltage V_{k1} drops to zero with the time constant

$$\tau_2 = R C \quad (4.57)$$

Fig. 4.55b shows the voltage waveform at tubes 1 and 2 (the burning voltage of the tubes can be regarded as approximately constant). The further rise of voltage V_{a1} at the extinguished tube should not occur too quickly so that there is no question of re-igniting tube 1 because of the charge carrier still present (see Section 3.9), i.e. the time constants τ_1 and τ_2 must be sufficiently large in relation to the recovery time. Moreover, it must also be borne in mind that the voltage at the trigger electrode follows the cathode voltage, delayed on account of the resistance R_T and the coupling capacitor C_T , so that there is still a dependence on the internal resistance of the source of the counting pulses. These influences limit the maximum counting speed of the circuit. We see that this limit is not only dependent on the tube but also on the component values in the circuit.

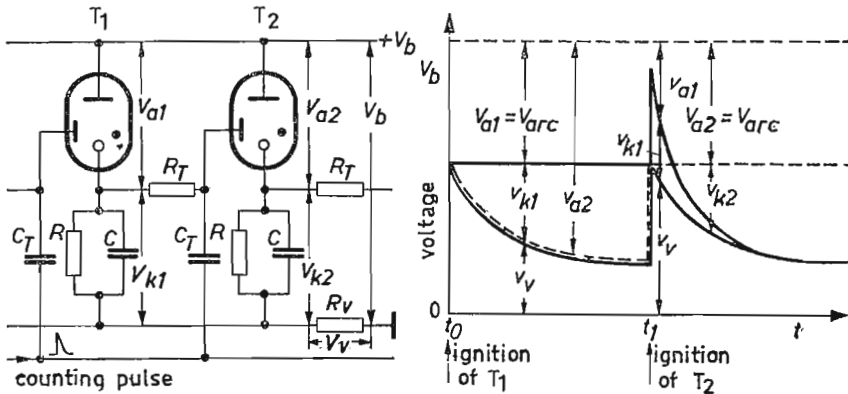


Fig. 4.56 Two elements of a ring counter with common cathode resistance

A suitable circuit can also be constructed with a common resistance R_v in the negative line of the feed voltage, as is shown in Fig. 4.56. After the first tube is ignited, the voltage V_{k1} increases at the cathode resistance R with the time constant

$$\tau_1 = \frac{R R_v}{R + R_v} C \quad (4.58)$$

to the end value

$$V_{k1} = (V_b - V_{arc}) \frac{R}{R + R_v}$$

This value must again be less than the trigger ignition voltage. When tube 2 is ignited, resistance R is short-circuited in the first instant, and a current

$$I_{a0} = \frac{V_b - V_{arc}}{R_v}$$

flows and tube 1 is only at voltage

$$v_{a1} = V_{arc} - V_{k1}$$

The voltage V_{k1} then drops to zero with the time constant

$$\tau_2 = R C \quad (4.59)$$

The rise again of the voltage between the anode and cathode of tube 1 then takes place according to the equation

$$v_{a1}(t) = \left[V_{arc} + (V_b - V_{arc}) \frac{R}{R + R_v} \right] \times \\ [1 - e^{-t/\tau_1} - e^{-t/\tau_2} + e^{-t/\tau_1 + t/\tau_2}]$$

The comments made above hold again for the choice of component values and the counting speed.

A third method of coupling illustrated in Fig. 4.57, corresponds in all respects to the trigger circuit (see Section 4.2.2) but it is made up into a ring counter with further tubes. Here it is only necessary to note that the cathode voltage jump at the ignition of a tube has to charge up not just one coupling capacitor but those of the entire ring, which raises the time constant.

Concerning selection of the values of R_T , C and C_T , the following must be said with regard to the above recommendation: The value of resistance R is fixed on account of the statements already made. Capacitor C , however,

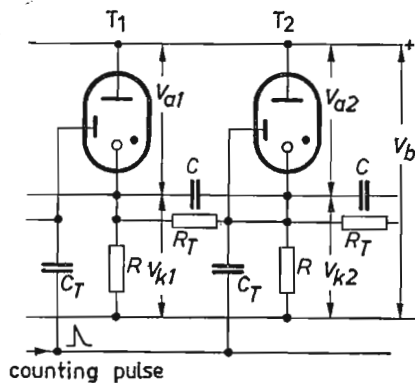


Fig. 4.57 Cathode-coupled ring circuit

must not be chosen too small, so that the voltage between anode and cathode does not rise too quickly, and the tube remains safely extinguished. On the other hand, it must not be too large, so that charging and discharging do not proceed too slowly. This would reduce the maximum counting speed. The most favourable value is best calculated by experiment. Resistance R_T and capacitor C_T should be chosen as large as possible, on one hand, so that there is no unnecessary distortion of the counting pulse, though on the other hand, there is again the limitation that the maximum counting speed would be reduced if the charging and discharging of capacitor C_T lasted too long. We reach a useful compromise if we choose

$$R_T C_T \approx RC$$

Fig. 4.58 shows a simple example for a counting decade with the relay tube Z 70 U. The build-up of the stages corresponds to the circuit in Fig. 4.57.

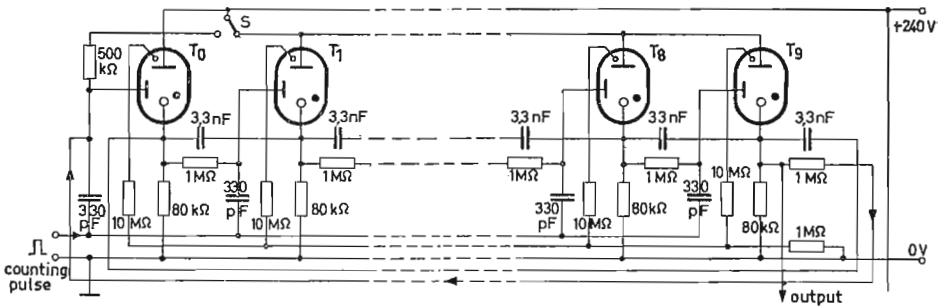


Fig. 4.58 Decade ring counter with Z 70 U (cathode-coupled)

Before the start of each counting operation, switch S must be momentarily set to the left. This brings the apparatus into the zero position by igniting tube 0 and extinguishing any of the other ignited tubes. The first counting pulse then ignites tube 1 and extinguishes tube 0. Tube 0 is again ignited by the tenth pulse; at the same time tube 9 is extinguished and an output pulse occurs at its cathode.

As a further example, Fig. 4.59 shows a decade counter with biquinary coding (see Fig. 2.14). Here the coupling of the stages is brought about through the common cathode resistance R_7 , according to the principle illustrated in Fig. 4.56. A trigger circuit consisting of tubes 6 and 7 coupled by a common resistance R_8 is used here as a bistable element M_1 (in Fig. 2.14). A further tube 8 serves as the pulse former for the output pulse. The counting process is as follows: By momentarily switching S over, the circuit is brought into zero position. Tubes 1 and 6 are conducting. The first counting pulse

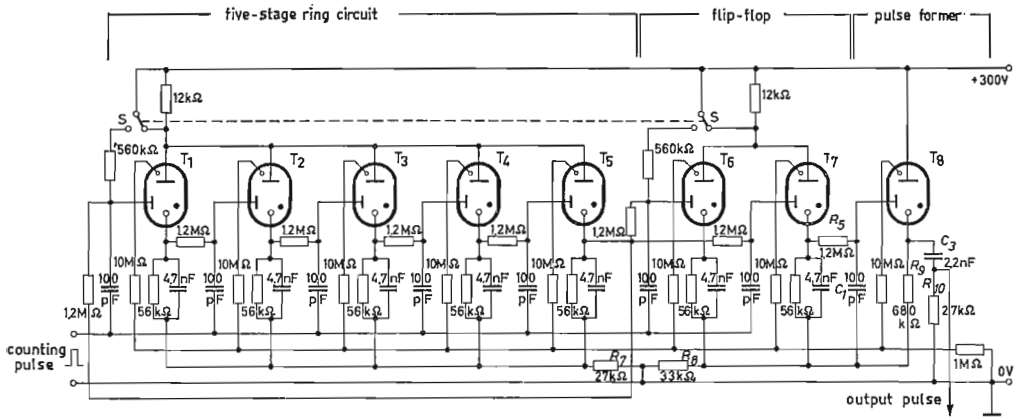


Fig. 4.59 Circuit of a biquinary counting decade with trigger tubes Z 70 U

ignites tube 2 and extinguishes tube 1; tube 6 continues to carry current. Tubes 7 and 1 are only ignited on the arrival of the fifth pulse, and at the same time, tubes 6 and 5 are extinguished. Now the five-stage ring is traversed afresh until the tenth pulse extinguishes tubes 5 and 7 and simultaneously ignites tubes 1, 6 and 8. The ignition of tube 8 is brought about under the following conditions: As long as tube 7 carries current, C_1 is charged up via R_5 . When tube 6 is ignited there is an erratic increase in the voltage drop at R_8 which leads to a rise of the trigger voltage of tube 8; this only slightly alters the cathode potential of tube 8, since the cathode is earthed via C_3 and R_{10} ($R_{10} \gg R_9$). There is thus an additional rise of voltage between trigger and cathode so that tube 8 ignites. In the first instant after ignition, capacitor C_3 acts as a short-circuit through which the effective cathode resistance is predominantly governed by R_{10} , and a voltage drop occurs at R_{10} which can be used as output pulse. After capacitor C_3 is charged, only R_9 is essentially effective as a cathode resistance. This resistance is so chosen that the current flowing through it is not enough to maintain the discharge. For that reason, tube 8 is quickly extinguished again and C_3 is almost fully discharged until the arrival of the succeeding tenth pulse via R_8 , R_9 and R_{10} .

A maximum counting speed of about 3 kc/s can be obtained with this circuit. This value is not an absolute limit. It can be raised, for instance, by applying a resistance of 8 kΩ in series with an inductance of 0.2 to 0.3 H in place of the resistance R_1 . The counting pulse at the input of the circuit should be about 15 to 30 μs long with a pulse strength of about 80 V.

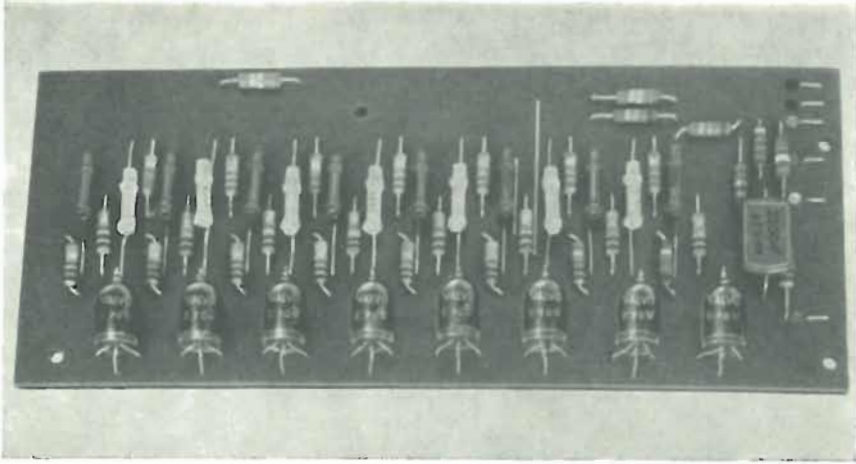


Fig. 4.60 Biquinary decade counter according to the circuit in Fig. 4.59

4.3.3 DECADE COUNTER WITH TRANSISTORS

As with tube circuits, counters can also be constructed with transistors as binary chains with four bistable multivibrators. Here again it is necessary to ensure by suitable feedback that the counter can only receive 10 of the 16 possible positions, thus omitting 6 positions. Experience shows [34] that the attainable counting speed with counters of this type is about

$$f_{max} \approx 0.2 f_{av}$$

where f_{fall} is the limiting frequency of the transistor used in the base circuit. The maximum counting speed is limited by the time needed to pass over the six surplus positions. For this reason we aim at the simplest possible feedback with little delay.

Fig. 4.61 shows an example of the connection of the four bistable stages to the decade counter. The coupling between the consecutive stages is such that only the output pulse produced at the switch-over from the L- into the O-position can switch over the next stage.

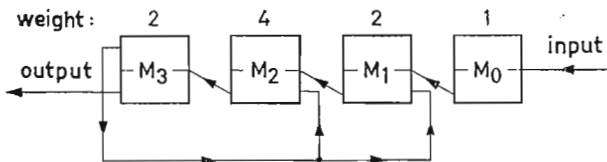


Fig. 4.61 Coupling the four stages

The counter counts binary up to and including "7" (OLLL) (see Table 2.3). The eighth pulse at first brings M_0 , M_1 and M_2 into the O position and M_3 into the L position. The output pulse thus produced at the other element of M_3 subsequently triggers over the stages M_1 and M_2 into position L again over the feedback lines, so that now the "8" (LLLO) is in the counter. The individual multivibrators are only switched over through positive pulses at the base of one of their transistors. By differentiation of the negative output pulses, the rear flank thus switches the multivibrators over so that the double switch-over of stages M_2 and M_1 takes place with sufficient delay. The circuit of the individual bistable multivibrators corresponds to Fig. 4.43. Fig. 4.62 shows the complete circuit diagram of the counter. Dimensioning for transistor types OC 71 and OC 46 is given in Table 4.7.

TABLE 4.7: DIMENSIONING OF CIRCUIT IN FIG. 4.62

Transistors	D	R_1 k Ω	R_2 k Ω	R_B k Ω	R_C k Ω	R_E k Ω	R_S k Ω	R_T k Ω	C_R pF	C_T pF	C_1 pF
OC 71	OA 81	15	47	10	3.3	3.3	1	8.2	600	2000	1000
OC 46	OA 91	11	56	10	3.3	3.3	1.2	8.2	200	300	200

Scattering can amount to $\pm 5\%$ for the resistances and $\pm 10\%$ for the capacitors. Table 4.8 gives the operational data for mounting the counter with types OC 71 and OC 46.

TABLE 4.8: OPERATIONAL DATA FOR COUNTER IN FIG. 4.62

Transistor	Input pulse		Max. ambient temperature $^{\circ}\text{C}$	f_{max} kc/s
	V	μs		
OC 71	+ 4	$\cong 2$	+ 45	35
	- 4	$\cong 20$		
OC 46	+ 4	$\cong 0.4$	+ 45	170
	- 4	$\cong 2.5$		

The counter can be returned to zero from any position through a switch which, by operating the resistances R_2 disconnects all the left-hand transistors. The return movement can be achieved electrically through a negative pulse V_R which goes through diodes D to the bases of all the left-hand transistors, as is shown in Fig. 4.62. The return line is normally at +1 V and must be brought to -4 V for the return movement. To avoid the delay (about 20 μs with the OC 71 and 3 μs with the OC 46) between the tenth input pulse

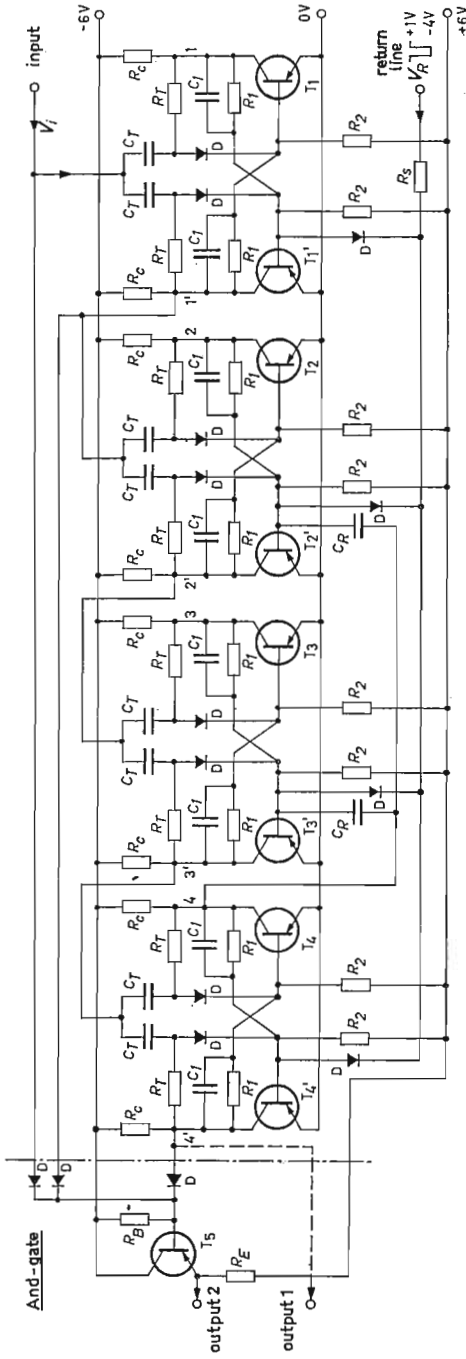


Fig. 4.62 Decade counter with RC coupling (for values see Table 4.7)

and the output pulse of the counter, an And-gate can be used. In this two inputs in position "9" of the counter are at transmission voltage through the stages M_0 and M_3 . The tenth pulse can then reach the output of the counter directly via the third input of the And-gate. The And-gate, consisting of three diodes with connected resistance transformer T_5 (OC 71 or OC 47) is likewise included in Fig. 4.62.

The counting speed can be raised by transformer coupling between the individual stages and by avoiding over-control of the transistor. Fig. 4.63 shows the block diagram of a counter constructed in this way. The suppression of the 6 surplus positions is done through an And-gate with three inputs. Inputs B and C of the gate are for a time at one output of stages M_2 and M_3 , and the input pulses effective at input A are only passed when the multivibrator M_2 is in the "L" position and multivibrator M_3 is in the "O" position. The counting process then goes as follows: Up to the fourth pulse is binary counted (see Table 2.3). During the first three pulses the And-gate is then blocked since inputs A and C lie at different voltages.

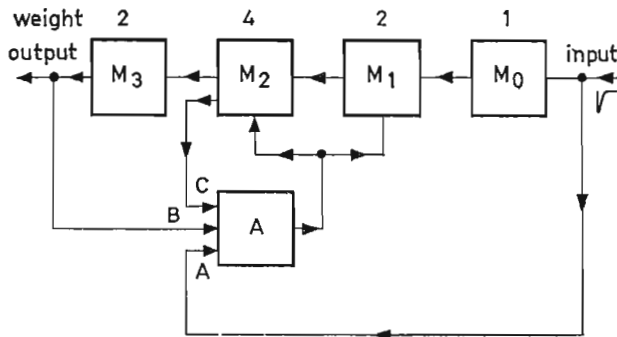


Fig. 4.63 Coupling of four stages (Aiken coding)

The fourth pulse brings the counter into position OLOO and thus opens the And-gate. The fifth pulse therefore additionally switches over stages M_1 and M_2 so that the counter condition LOLI is now obtained. In place of the binary five, the binary eleven is produced; the counter has jumped over 6 positions. The remaining 4 pulses are again counted normally since the And-gate now remains closed because of the "L" in M_3 . The tenth pulse finally brings the counter back to the zero position. The indication of the counter condition is done in this way in the Aiken coding (see Section 2.2.2). The positions of the individual stages in Fig. 4.63 correspond to Table 2.1; the values are successively 1, 2, 4 and 2.

Fig. 4.64 shows the circuit of the multivibrator used.

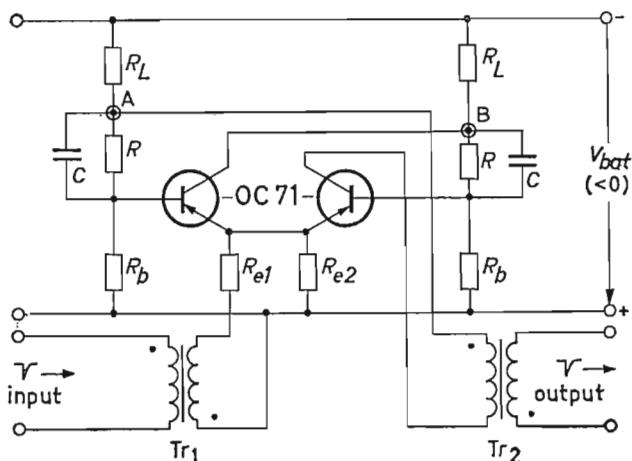


Fig. 4.64 Bistable multivibrator (for values see Fig. 4.67)

The coupling of the individual stages is done here via small transformers with Ferroxcube cores. When the left transistor in Fig. 4.64 is conducting and the right one is blocked, the emitter voltages of both transistors are negative through a negative pulse at the input. The conducting transistor is thus blocked and the triggering over of the circuit is begun in the familiar way. In this manner each negative pulse at the input causes the switch-over of the stage, no matter which of the two transistors is blocked. The square-wave voltage thus produced is differentiated in the transmitter so that two pulses of opposite polarity are yielded at the secondary. The multivibrator, however, only reacts to negative pulses.

With appropriate dimensioning of the multivibrator, the opened transistor is not controlled as far as the bend X (Fig. 4.65), but only as far as point X' (about -3.9 V). A positive pulse at the emitters of the two transistors thus raises the collector current of the opened transistor (X' moves in the direction of X). The reduction of its collector voltage produced in this way operates via the coupling capacitor C at the base of the blocked transistor as a positive pulse, which makes the positive pulse at the emitter ineffective. This transistor thus remains blocked (the positive pulse voltage may amount to 40 V without initiating the triggering process). At the same time, through the setting of the working points, the stability of the stage is increased against spreads in the transformers as well as against fluctuations of the feed voltage. With a feed voltage fluctuation of $\pm 50\%$, the multivibrators still operate satisfactorily up to 100 kc/s switch frequency. The control of the emitter of the transistor takes place as current control via the secondary windings of the transformer.

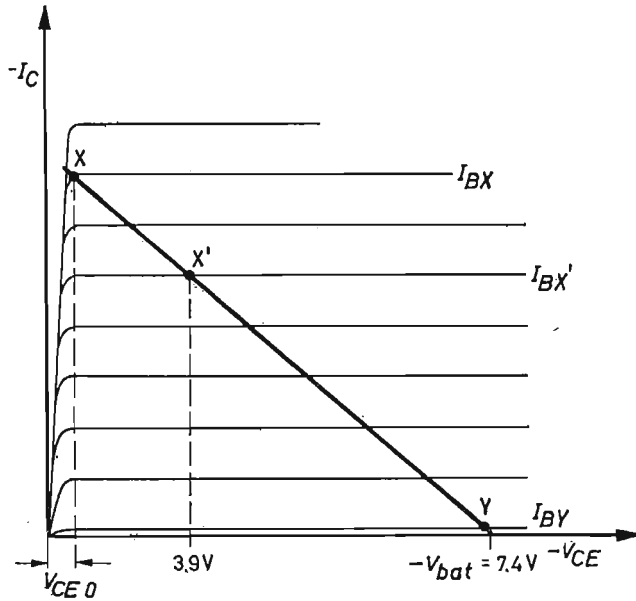


Fig. 4.65 Working points X' and Y of the transistors in the circuit of Fig. 4.64

The resistance which limits the current consists of R_{e1} and R_{e2} . The d.c. resistance effective for the emitter itself is composed of the parallel circuit of both resistances (330Ω). This resistance means a very effective d.c. stabilising in the face of temperature influences and component spreads.

Fig. 4.66 shows the circuit of the And-gate in Fig. 4.63. This is open when

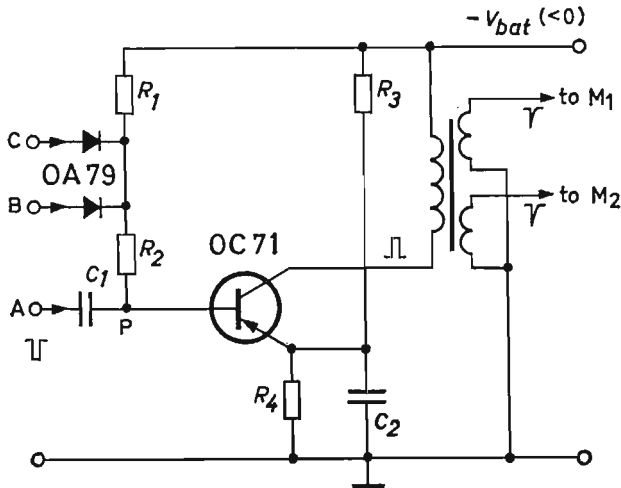


Fig. 4.66 Circuit of the And-gate (for values see Fig. 4.67)

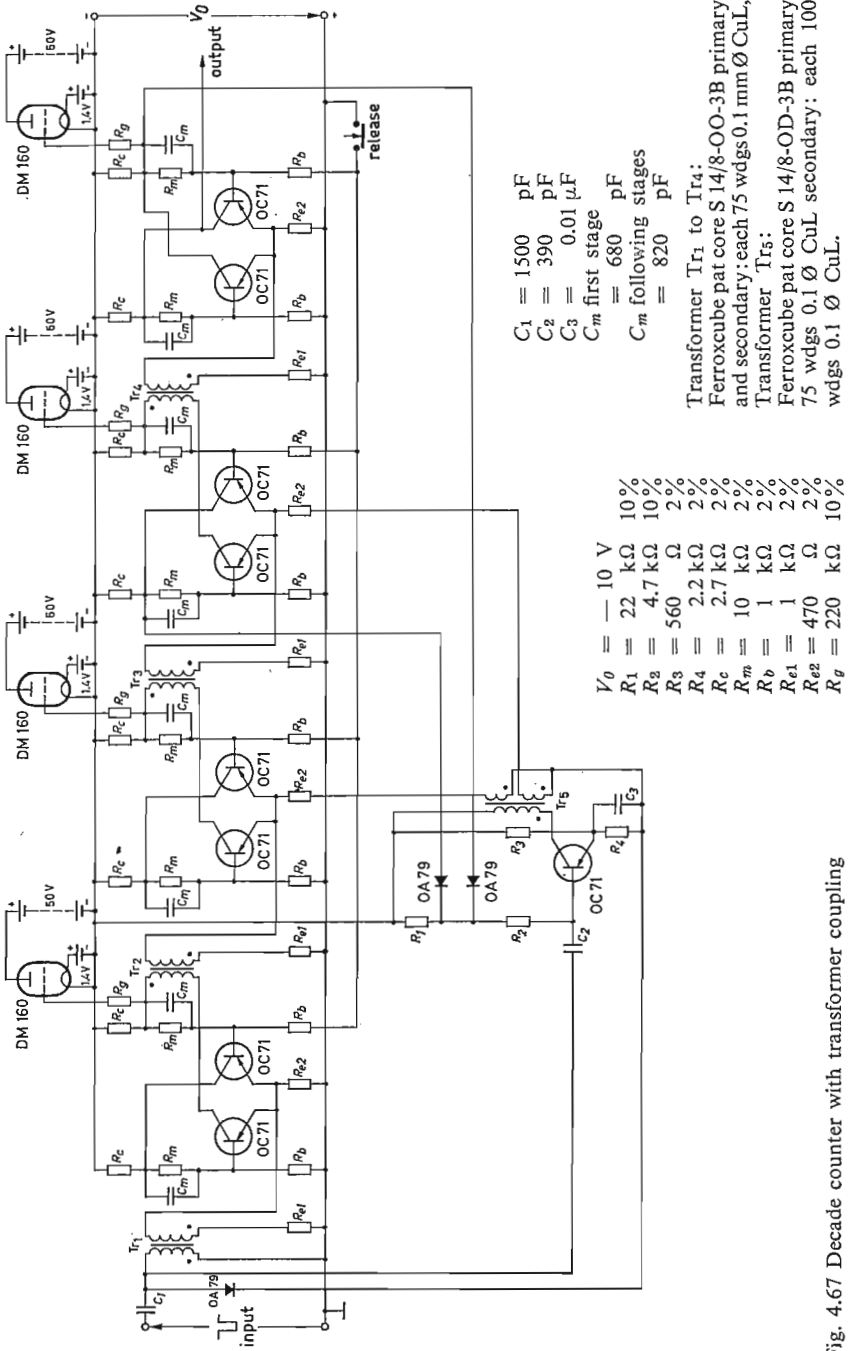


Fig. 4.67 Decade counter with transformer coupling

inputs B and C are at the collector voltage of the corresponding blocked transistor (-8 V below earth) in stages M_2 and M_3 .

The emitter of the transistor serving as pulse amplifier in the gate lies at -8 V so that the transistor is still blocked up to -8 V. If the small collector voltage of the opened transistor (-4.5 V below earth) is at input B or C or at both, point P is fixed through at least one diode at the collector voltage of the opened transistor, and a negative pulse below 4.5 V at input A cannot open the transistor. Only if B and C are at -8 V does the input pulse at A open the transistor and produce in both secondary windings of the output transformer the two pulses for switching over stages M_1 and M_2 .

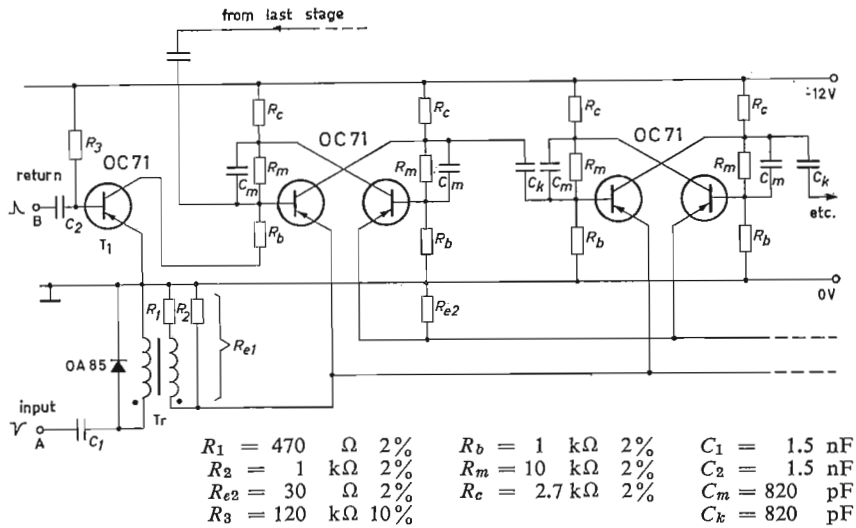
Fig. 4.67 shows the complete circuit of the decade counter. There is also a diode at the input to cut off any possible positive pulses. The base resistances of all the right-hand transistors are connected to one push-switch. As soon as this is opened, all the right-hand transistors are conducting, i.e. the counter jumps back to the zero position and the counting result is cleared. If a visual indication of the counter condition is desired, this can be accomplished with the small tuning indicator tube DM 160. As soon as the left-hand transistor is conducting, the grid of the accompanying DM 160 is positive and the tube lights up. The counter condition is indicated in this way in the Aiken coding.

The counting unit works with negative input pulses (square-wave pulses) of at least 1.8 V with a minimum pulse duration of $2 \mu\text{s}$. The output pulse amounts to about 3.5 V at no-load. The maximum counting frequency is about 85 kc/s. The working method is not affected by feed voltage changes up to $\pm 15\%$. The power consumption (without indicator tubes) amounts to 140 mW. With the use of printed wiring the whole equipment can be accommodated in a space of $12 \times 10 \times 0.8$ cm. This is about 10% of the space needed by a similar equipment with electronic tubes. On account of the extra input load through the And-gate, several decades of intermediate amplifiers must be connected in a series circuit.

4.3.4 RING COUNTER WITH TRANSISTORS

By suitably coupling ten bistable multivibrators, it is easy to construct a ring counter corresponding to Fig. 2.13 with transistors. Here the individual bistable elements must have the properties described in Section 2.4.3.2.

Fig. 4.68 indicates two stages of this kind of ring counter. The individual multivibrators are coupled from the collector of the left-hand transistor of one stage to the base of the left-hand transistor of the following stage via C_k . All the left-hand and all the right-hand transistors each have a common emitter resistance (R_{e1} and R_{e2}). A negative pulse at input A makes the



Transformer Tr:

Ferroxcube pat core S 14/8-00-3B, each 75 wdgs 0.1 mm \varnothing CuL (all resistances 1/8 W, all capacitors ceramic)

Fig. 4.68 Two bistable elements and return stage of a ring counter

emitters of all the left-hand transistors negative so that these are blocked. The condition of a stage: left-hand blocked, right-hand conducting should correspond to the position "0", the reverse condition to the position "L". If, for example, the first stage is in position "L", then an input pulse at the emitters of all the left-hand transistors produces a negative pulse which switches the first stage over into position "0". This switch-over produces via C_k a negative pulse at the second stage and triggers this into position "L" provided its effect sufficiently exceeds the influence of the negative pulse at the emitter. The positive pulse now yielded by the second stage has practically no effect on the third stage as this is in position "0". With the next pulse the digit "L" again moves one place to the right and so on. The working method of the circuit is not altered even if the last stage is coupled again to the first.

The return of the ring counter from any chosen position to the zero position ("L" in the first stage) can be brought about in the following way: The base resistance R_b of the first stage is not directly earthed but via transistor T_1 which is normally opened through R_3 . T_1 , however, is blocked by a small positive pulse at input B through which the base of the left-hand transistor of the first stage gets a negative voltage and is switched into position "L". The stage previously in position "L" in any place of the counter is thus brought to "0" via the common emitter resistance R_{e1} .

In the ring counter described, one of the left-hand transistors is always conducting and $n-1$ blocked, while $n-1$ of the right-hand transistors are conducting and one is blocked. In this way different currents flow over the two common emitter resistances. The ratio of the emitter resistances must then amount to

$$\frac{R_{e1}}{R_{e2}} = n - 1$$

In this ring counter, care must be taken with the coupling since the opened transistor is not completely conducting and the blocked one is not entirely without current. The extent of the continuing effect at switching of the small pulses thus produced in the ring mainly depends on how strongly the voltage changes still influence the stage which follows the switched-over stage. Experience shows that a repeated "blocking" of a blocked transistor results in a smaller pulse than "opening" an already open transistor. This has been taken into account in the coupling of the individual stages in Fig. 4.68. Here the left-hand blocked transistor of one stage is "blocked" once again. The small pulse arising at the collector is not enough to open the left-hand transistor of the following stage. The ring counters operate at temperatures up to 60 °C with 50 kc/s maximum counting frequency.

In view of the spreads of the transistors and resistances, the number of stages is limited in the ring counter described above because of the common emitter resistance. The common emitter resistance can nevertheless be avoided by appropriate coupling of the individual bistable multivibrators [86]. The number of stages is then practically unlimited. Fig. 4.69 shows the basic circuit of a bistable multivibrator suitable for this. The circuit is marked by the fact that it has three release inputs: the common input E_1 , the input 1b for the right-hand transistor and input 1'b for the left-hand one. Let us suppose that the left-hand transistor T_1' is switched on at first and is thus over-controlled. The right-hand transistor T_1 is then switched off. Since the emitters of both transistors are at zero, the collector potential of T_1' is equal to the residual voltage V_{CE0} of an over-controlled transistor, and in this circuit amounts to a maximum of -0.3 V. As a result of the over-control of the transistor, the corresponding base voltage is somewhat more negative than the residual voltage and lies at a maximum of -0.35 V. Collector 1 of the blocked transistor T_1 is at about -4.8 V. The base voltage of the blocked transistor T_1 is sufficiently positive and even in unfavourable ratios lies above $+0.2$ V. There is thus a blocking voltage of at least -5 V at the diode D_T which lies between the input (E_1) and the base of T_1 and which is connected

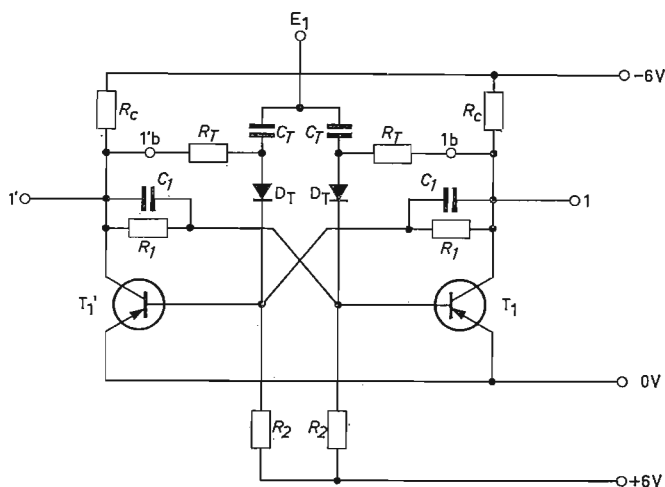


Fig. 4.69 Basic circuit of a bistable stage

to the collector via a resistance R_T . The diode leading to the base of the switched-on transistor T_1' , on the other hand, is slightly biased in the transmission direction since the collector of an over-controlled transistor is positive towards the base.

If a positive release pulse with steep sides and an amplitude of less than 5 V is given at the common input E_1 , it will be conveyed directly to the base of T_1' via the diode biased in the transmission direction, while the path via the diode of T_1 biased in the blocking direction is cut off. In this way, the blocking of T_1' is introduced through the positive release pulse and the multivibrator is switched over into its other position. The bias potentials of the two diodes are exchanged at the switch-over so that a subsequent positive release pulse triggers the stage again into the initial condition. The switch condition of the multivibrator stage “ T_1' conducting, T_1 blocked” should, in the following, correspond to the “0”, the condition “ T_1' blocked, T_1 conducting” to the “L”. If the input has a negative square-wave pulse, this is then differentiated by C_T and R_T . In this way, only the positive portion yielded by the rear flank can be effective for switching over the stage. While the switching over takes place at the leading edge when the stage is controlled by positive pulses, it now begins at the rear flank. (Delay circuits can often be avoided in this way.)

If a ring counter is to be constructed with multivibrators of this type, the bias potentials of the diodes D_T must be controlled by the preceding stage.

Points 1b and 1'b therefore do not lie at the collectors of their own stage but at those of the previous stages, as is shown in Fig. 4.70 in the example of a three-stage ring counter: The left-hand collector of stage n controls the input of the right-hand stage $n + 1$, and the right-hand collector of stage n , the left-hand input of stage $n + 1$. The ring counter is closed by coupling 3' to 1b and 3 to 1'b.

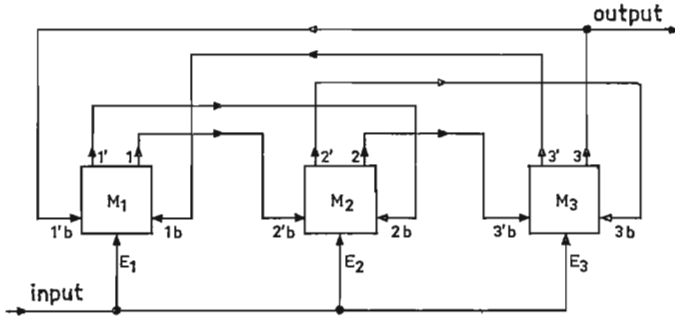
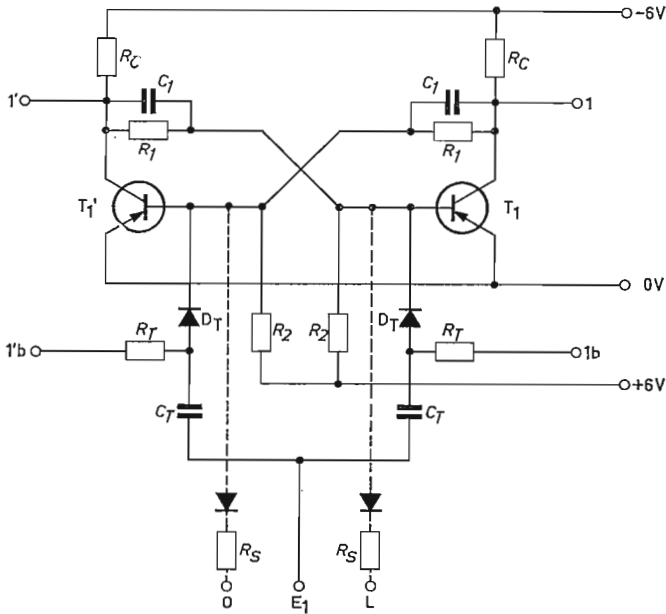


Fig. 4.70 Coupling of stages in a three-ring counter

Fig. 4.71 shows the complete circuit of a stage. As well as the inputs E_1 , 1b and 1'b already mentioned, the two inputs 0 and L are also included. Through a negative voltage, these make it possible to return a stage from "0" or to set it at "L". Since these two inputs are the same for all stages in the ring counter, they have to be decoupled by additional diodes. Inputs 0 and L must be at a positive rest voltage of at least $+0.5V$ approximately. The resistances R_s should attenuate the load reactions on the voltage sources. The value of R_s should be greater than the transmission resistance of the diode and should be so selected that with a given negative control voltage, the negative current flowing into the base to switch on the transistor concerned is $\geq 0.7 \text{ mA}$. The multivibrator can still be set within a maximum of $6 \mu\text{s}$, under this proviso, through a negative pulse with a rising time of $\leq 0.5 \mu\text{s}$. The setting is quicker with greater values of the setting-current. The following summary gives the maximum attainable operational values for a ten-stage ring counter.

Two working methods are given, one with narrow positive control pulses and the other with square-shaped negative control pulses. The latter method is chiefly of importance in the possible use of And-gates for additional control purposes. The working values given have a good safety margin. They have been obtained under unfavourable combinations of resistance



$$\begin{aligned}
 R_C &= 3.3 \text{ k}\Omega \pm 5\% \\
 R_1 &= 15 \text{ k}\Omega \pm 5\% \\
 R_2 &= 47 \text{ k}\Omega \pm 5\% \\
 R_T &= 8.2 \text{ k}\Omega \pm 5\%
 \end{aligned}$$

$$\begin{aligned}
 C_1 &= 1000 \text{ pF} \pm 10\% \\
 C_T &= 2000 \text{ pF} \pm 10\% \\
 T_1, T_{1'} &= \text{OC 71} \\
 D_T &= \text{OA 81}
 \end{aligned}$$

Fig. 4.71 Design of a stage in the ring counter of Fig. 4.70

tolerances as well as normal transistor characteristic values (e.g. static current amplification $\bar{a}_\theta \geq 24$; $-I_{CB0} \leq 5 \mu\text{A}$ at $+25^\circ\text{C}$); at the same time, working voltage fluctuations (change in the same direction of $V_{bat1} = -6 \text{ V}$ and $V_{bat2} = +6 \text{ V}$) are permissible to a maximum of $\pm 10\%$. The maximum ambient temperature can amount to $+45^\circ\text{C}$.

a) Operation with positive control pulses

Control source: Pulse generator with an internal resistance $R_g \leq 50 \Omega$.

Input without impedance transformer.

Pulse amplitude: $6 \text{ V} \geq V_t \geq 4 \text{ V}$

Pulse duration τ : $3 \mu\text{s} \leq \tau \leq 5 \mu\text{s}$

Minimum counting pulse resolving times (interval between two pulses):
 $\geq 30 \mu\text{s}$

With periodic pulse operation this corresponds to a maximum pulse frequency of about 30 kc/s.

b) *Operation with negative control pulses*

Control source: Pulse generator with an internal resistance $R_g \leq 1 \text{ k}\Omega$.

Input with resistance transformer

Pulse amplitude: $6 \text{ V} > -V_t \geq 4 \text{ V}$

Pulse rising and falling time: $t_{rise}, t_{fall} \leq 5 \mu\text{s}$

Pulse duration: $\tau \geq 30 \mu\text{s}$

Minimum counting pulse resolving times: $12 \mu\text{s}$

The permissible load of the individual collectors in the ring counter may amount to a minimum of $3.3 \text{ k}\Omega$ for the switched-on transistor, and for the blocked transistor about $40 \text{ k}\Omega$ against $+6 \text{ V}$ and $15 \text{ k}\Omega$ against 0 V .

4.4 Store and register

Storage circuits can be constructed with tubes, transistors and square-loop ferrite cores. The square-loop ferrites are used in great numbers for storage purposes, while tubes and transistors are generally only employed in small stores and registers (stores for one word) on account of the expense.

4.4.1 DECIMAL REGISTER WITH TRANSISTOR COUNTERS

In Section 2.6.2 the working method was described of a store for one decimal number, consisting of two counters and a logical circuit (see Fig. 2.19). Here one counter serves for the actual storing while the other operates as a 1:10 frequency divider and, together with the logical circuit composed of a bistable multivibrator and an And-gate makes the series reading of the stored digit possible.

Fig. 4.72 shows how this kind of store can be realised with transistor circuits. The circuit described in Section 4.3.3 is used for the counter x and the frequency divider. A pulse amplifier is also provided for the writing pulses. The counters themselves are merely shown as blocks; only the somewhat modified input of counter x is indicated. The outputs of the counter go over the same coupling transformers as will be used between the individual stages.

Here we use two multivibrators and two And-gates with three inputs for the logical circuit, as is shown in Fig. 4.73. In the block diagram of Fig. 2.19 it consisted of one multivibrator and one And-gate. In this way the two multivibrators only need to be released via one input at a time. In the rest position both multivibrators are in the odd condition (upper transistor in Fig. 4.73 blocked). The And-gates only pass the clock pulses at A_1 and A_2 when inputs B_1 and C_1 or B_2 and C_2 lie at the collector voltages of the blocked transistors in M_1 and M_2 (-8 V); thus, both gates are blocked at

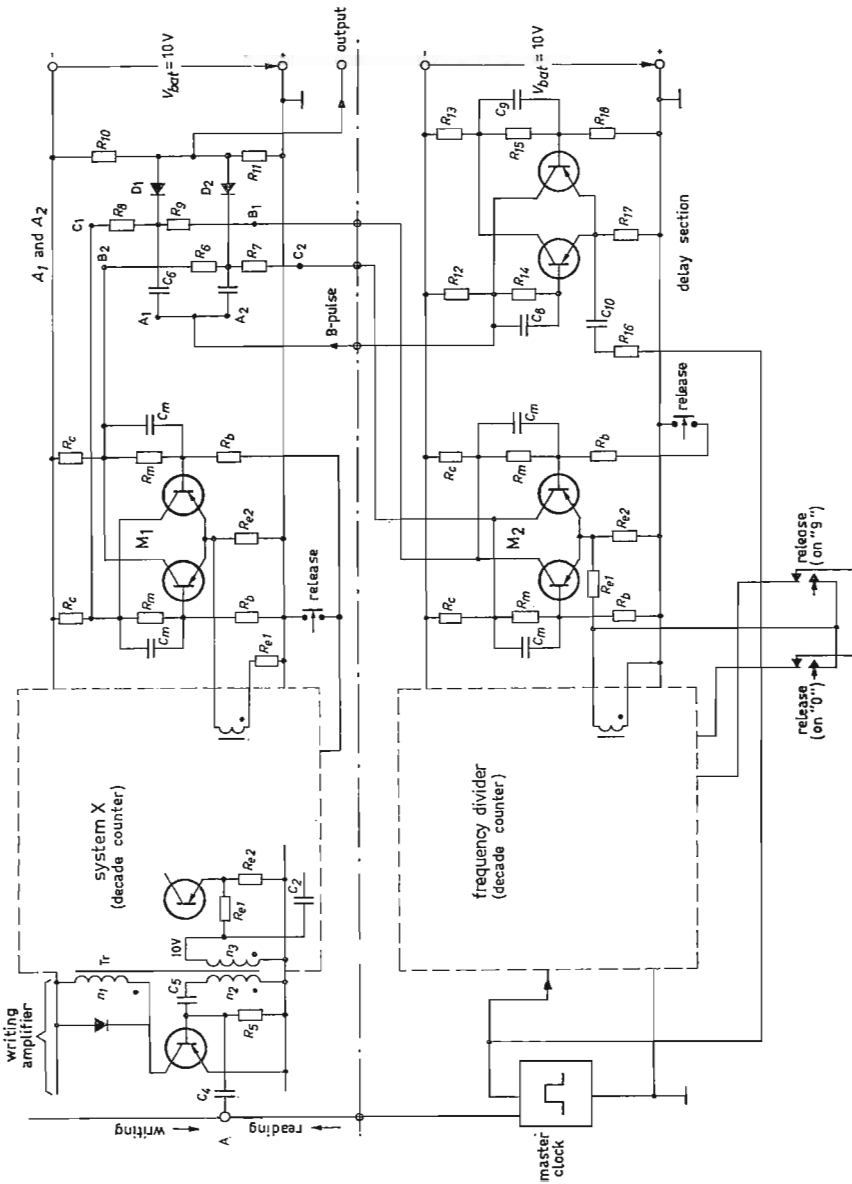


Fig. 4.72 Circuit of a store for a decimal figure (for values see Table 4.9)

TABLE 4.9: COMPONENT VALUES OF THE CIRCUIT IN FIG. 4.72

$R_c = 2.7 \text{ k}\Omega$ 2%	$R_{10} = 47 \text{ k}\Omega$ 2%
$R_m = 10 \text{ k}\Omega$ 2%	$R_{11} = 220 \text{ k}\Omega$ 2%
$R_b = 1 \text{ k}\Omega$ 2%	$R_{12} = 2.7 \text{ k}\Omega$ 2%
$R_{e1} = 1 \text{ k}\Omega$ 2%	$R_{13} = 2.7 \text{ k}\Omega$ 2%
$R_{e2} = 470 \text{ }\Omega$ 2%	$R_{14} = 470 \text{ k}\Omega$ 10%
$R_5 = 1 \text{ k}\Omega$ 10%	$R_{15} = 10 \text{ k}\Omega$ 2%
$R_6 = 56 \text{ k}\Omega$ 10%	$R_{16} = 1 \text{ k}\Omega$ 10%
$R_7 = 56 \text{ k}\Omega$ 10%	$R_{17} = 330 \text{ }\Omega$ 2%
$R_8 = 56 \text{ k}\Omega$ 10%	$R_{18} = 1 \text{ k}\Omega$ 2%
$R_9 = 56 \text{ k}\Omega$ 10%	(all resistances $1/8 \text{ W}$)

C_m for M_1 and $M_2 = 1500 \text{ pF}$	
$C_4 = 1500 \text{ pF}$	(all resistances $1/8 \text{ W}$)
$C_5 = 1500 \text{ pF}$	Germanium diodes: OA 70
$C_6 = 33 \text{ pF}$	Transistors : OC 71
$C_7 = 33 \text{ pF}$	Transformer T_r : Shell core S 14/8-00-3B
$C_8 = 120 \text{ pF}$	
$C_9 = 180 \text{ pF}$	
$C_{10} = 1500 \text{ pF}$	

(all capacitors ceramic) Remaining component as in Fig. 4.67

first. Pulse P_x from the counter puts M_1 into the even condition through which gate A_1 becomes conducting, since -8 V now lies at B_1 and C_1 . The tenth pulse P_0 triggers M_2 over so that A_1 is blocked again because of the small collector voltage at B_1 . If the reading is repeated, M_1 is again triggered into the odd condition through P_x . M_2 , however, is still in the even condition from the previous reading, so that -8 V lies at B_2 and C_2 and the x master-clock pulses go via A_2 to the output. In this way the reading can be repeated as often as desired.

The circuit of the multivibrators M_1 and M_2 corresponds to the bistable elements in the counters (Fig. 4.64). The method of operation of the gate

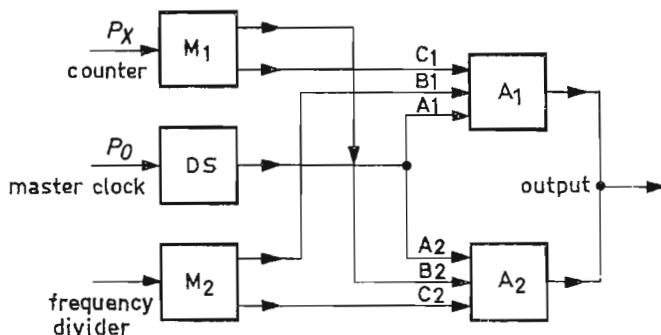


Fig. 4.73 Block diagram of the logical circuit

constructed with the diodes D_1 and D_2 is similar to the circuit described in Section 4.3.3 (see Fig. 4.66).

The delay stage DS of the clock pulses consists of a monostable multivibrator which, after a fixed time, triggers itself back into its original condition and thus yields an output pulse. The circuit of this stage can be seen in the complete circuit of Fig. 4.72. The left-hand of the two transistors is conducting in the resting condition; the right-hand one is blocked. A negative pulse arriving at the capacitor C_{10} at first produces no switch-over of the stage. When C_8 and C_9 are discharged, the multivibrator triggers back and a negative pulse is delivered at the gates.

The pre-amplifier stage is necessary for several reasons. It supplies the input amplitude needed for the decade counter (see Section 4.3.3) and produces the required flank steepness. It thus acts at the same time as a pulse former so that the input pulses at the counter, even when distorted, possess the required flank steepness. An amplitude of 1 V is thus sufficient for the input pulses. In the pre-amplifier we are dealing with a blocking oscillator which is blocked in the basic condition, for in the rest position its feedback factor is less than 1. As soon as a negative pulse arrives at the base, the current amplification increases and the blocking oscillator delivers an output pulse. The attenuation of the oscillation is damped by a diode.

As well as the base leakage resistances R_b (see Fig. 4.67) on the right-hand side, those on the left-hand side also are led from the frequency divider to a switch. This can bring the frequency divider into the "LLLL" position instead of the "0000", i.e. to the decimal digit "9". With this initial position the store then delivers, on reading, the nine-complement (see Section 2.3.1.1) of the stored digit.

The register shown in Fig. 4.72 has a power consumption of about 580 mW of which 160 mW are needed for the indicator tubes in the counters. The feed voltage here amounts to 10 V. A negative pulse of 1.8 V amplitude can be tapped at the output. The maximum pulse frequency is about 85 kc/s.

4.4.2 BINARY SHIFT REGISTER WITH TRANSISTORS [53]

The working method of the binary shift register has been mentioned in Section 2.7.1. It can be composed of a chain of bistable elements (see Fig. 2.35) connected together over delay sections; for an N -place word, N bistable elements and $N - 1$ delay sections are needed. The bistable elements must have two inputs, one for writing the digits, the other for the shift pulses.

Fig. 4.74 shows the circuit of a stage consisting of the bistable circuit, the delay line and a separator stage. A shift register constructed with this stage works with a maximum 100 kc/s pulse series frequency (digital or shift pulses).

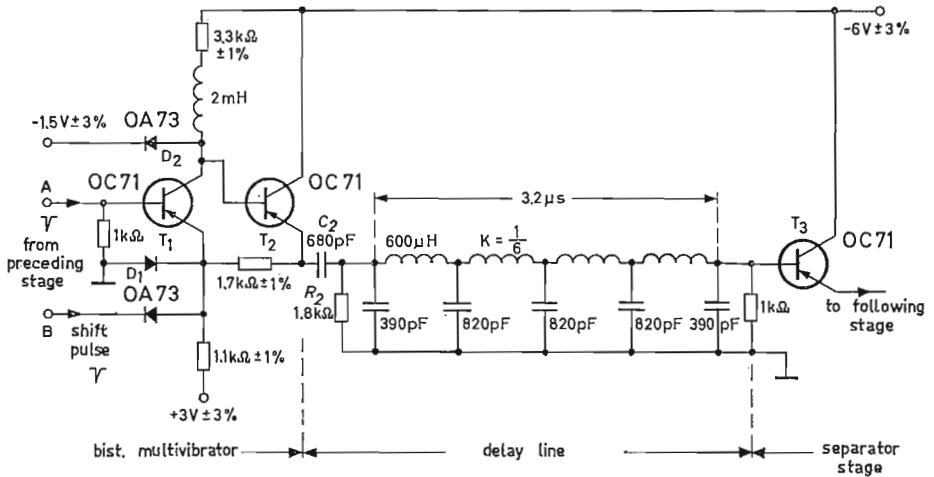


Fig. 4.74 One stage of a binary shift register

The bistable element consists of asymmetrical multivibrators. These offer the advantage that input and output do not lie in the feedback section, and the output is low resistance because of the collector circuit of transistor T₂. The output voltage alters according to the condition of the multivibrator between about -6 V (T₁ blocked, position "0") and -1.5 V (collector of T₁ at -1.5 V: position "L"). The two diodes increase the release sensitivity of the multivibrator and shorten the switching times. Diode D₂ prevents the over-control of transistor T₂ since it keeps the collector of T₁ at -1.5 V; this keeps the storing effect of T₂ small, for one thing, and for another, the transistor can more easily be blocked again. Diode D₁ limits the emitter potential of the blocked transistor T₁ to a small negative value and thus reduces the release amplitude required. The release of the multivibrator can take place at input A (digital pulse) and at input B (shift pulse). A negative pulse at A brings the multivibrator into position "L", and a negative pulse at B brings it back again to position "0". The switching time amounts to 4 μs, so that for the pulse at input A about -0.45 V and 0.75 mA are required, and at input B about 0.5 V with 2.1 mA. The switch delay (between application of the release pulse and the application of the output pulse of the multivibrator) is about 1 μs. The maximum switch frequency lies at 200 kc/s so that the digital or shift pulse series frequency can amount to a maximum of 100 kc/s.

The delay line consists of a four-section LC-chain whose delay time is calculated from

$$\tau = \sqrt{\Sigma L \times \Sigma C}$$

and whose characteristic impedance is deduced from

$$Z = \sqrt{\frac{\Sigma L}{\Sigma C}}$$

The output pulse of one stage may only arrive at the succeeding stage when the switching over is completed, i.e. after 4 μ s. Since the output pulse of T_2 is first differentiated (by C_2 and R_2) before it reaches the delay line, which takes about 1 μ s, the delay line only needs a minimum delay of 3 μ s. With the line used, the delay amounts to 3.2 μ s and the characteristic impedance is 1 k Ω . Its limiting frequency lies at about 500 kc/s which is sufficient for pulses with 2 μ s rise time.

The separator stage consisting of transistor T_3 in the collector circuit fulfils several functions:

- a) The suppression of the positive disturbing pulse which occurs when the stage is switched over by the shift pulse from "L" to "0" and which would disturb the next stage. In the rest position T_3 is almost blocked (base and emitter each lie at about 1 k Ω above earth) so that the positive pulse is virtually not passed.
- b) The high input resistance of the collector circuit allows the delay line with its characteristic impedance to be terminated (through the resistance of 1 k Ω).
- c) The transistor T_3 operates as a separator stage; it prevents the reaction of disturbing pulses from one stage on the preceding one.
- d) Finally, the separator stage brings about at the same time a pulse shaping of the pulses distorted in the delay line.

The ring counter shown in Fig. 4.70 can also serve as a shift register since it not only passes on an "L" but the condition of each stage containing an "L" [86]. The shift pulses are then passed to the input while the digital feed takes place through negative pulses over the (in this case separated) O- and L- inputs (see Fig. 4.71).

4.4.3 TRANSISTOR DRIVING STAGES FOR CORE STORES

Transistors are widely used as driving stages in core stores. The transistors have to supply the current pulses required to reverse the magnetisation of the type of storage core used, in which case the amplitude, the rise time and the duration of the pulses are significant (see Section 3.5.4). The transistors used here as switches must in general be made into current sources through extra series resistances, thus necessitating high collector voltages. Great demands

are therefore made on drive transistors, particularly on the maximum peak collector currents, the length of the switching time and the amount of storage effect and on the maximum permissible collector voltage. In view of the high current load of transistors in the switched-on condition, the value of the collector residual voltage and the collector leakage capacitance are important.

4.4.3.1 Switch current and temperature

The magnetic properties of storage cores are dependent on temperature. With rising temperature the output voltage increases and the switching time decreases at equal switch-over current. The optimum value of the switch current is moved to smaller values with increasing temperature (see Fig. 3.32). In the temperature range of general interest, between 25 °C and 50 °C, the optimum switch current, e.g. for the 6 D 3 core, decreases approximately linearly at about 3 mA per °C, i.e. a temperature fluctuation of $\pm 10\%$ alters the value of the optimum switch current by $\pm 5\%$.

To reduce the influence of temperature we can stabilise the temperature to some extent in core stores, or we give the driving current a suitable temperature coefficient so that the battery voltage decreases, e.g. by 0.5% per °C for the 6 D 3 core. Fig. 4.75 shows how this can be achieved in a simple manner through a transistor R_2 [75]. The collector feed voltage V_{bat}' is obtained through the voltage divider via R_1 and R_2 , whereby R_2 becomes smaller with rising temperature. The temperature dependence of the storage core can thus be greatly compensated by suitable choice of resistances.

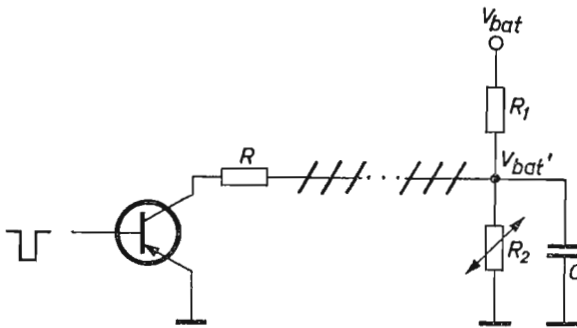


Fig. 4.75 Compensation of the temperature of storage cores by a thermista

4.4.3.2 Reducing the collector feed voltage

The permissible collector voltage of normal H.F. junction transistors is not sufficient for larger core stores on account of the voltage drop at the series

resistance required for current stabilisation (see Section 3.5.4.2). There are several measures which make it possible to reduce the collector feed voltage, some of which will be mentioned:

a) Using rectangular matrices instead of square ones

The distribution of the cores in the store is undertaken so that there are long columns and short lines. The column-driver transistors yield flat long pulses. The inductive counter-voltage then remains low in spite of the large number of cores. After reaching the end value of the column current, a short steep line pulse is then introduced. This supplies a high inductive counter-voltage for each core, though the number of cores for this is low. The disadvantage of this arrangement lies in the fact that the more the matrix form diverges from the square, the greater is the outlay at the driving stages for the same storage capacity. In addition, there are other important factors which fix the distribution of the cores in the matrix.

b) Current stabilisation by means of a diode

In cases where the voltage demand is given by the switched cores, — e.g. through the Relation (3.28) — the feed voltage can be considerably reduced, by means of a suitably biased diode, almost to the value of the maximum drop at the switched core. Fig. 4.76 shows the circuit. In the blocked condition of the transistor, diode *D* keeps the collector voltage at -6 V. As long as the voltage drop at the line remains more positive than -6 V after the transistor is switched on, the diode does not operate; -50 V then appears at the driving stage across the series resistance *R*. This can produce an almost 9-fold voltage drop.

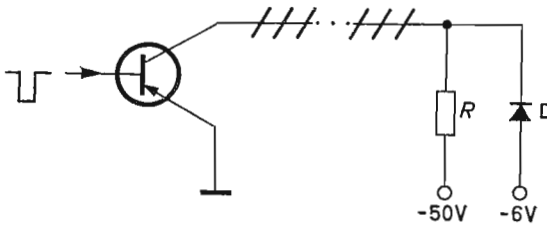


Fig. 4.76 Current stabilisation by means of a diode

c) Current stabilisation through non-linear resistances

A further possibility of reducing the collector voltage is the use of a non-linear resistance as the series resistor, i.e. the resistance must rise with in-

creasing current. Ferrite cores can also be used as series-connected chokes and their saturation can be utilised for current stabilisation [87].

d) Current stabilisation by reverse coupling

By applying the negative control pulse V_i to the circuit of Fig. 4.77, the collector current is given approximately by the relation

$$I_C \approx - \frac{V_i - V_{bat2}}{R_E}$$

as a result of the reverse coupling through the emitter resistance R .

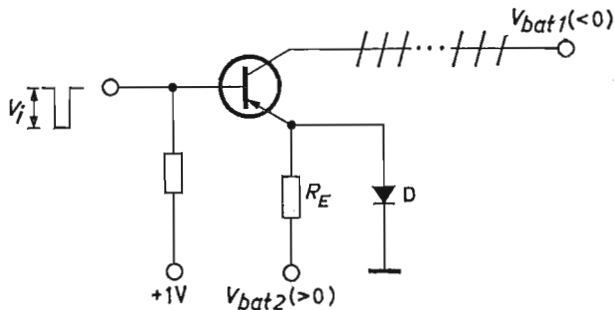


Fig. 4.77 Current stabilisation by reverse coupling

The collector current is largely independent of the collector voltage and the properties of the transistor. The voltage drop at the store can fluctuate between 0 and almost V_{bat1} without affecting I_C . In this way, the problem of current stabilisation is reduced to a constant input voltage V_i . The transistor works here, however, in the A-operation so that substantial collector leakage capacitances arise during the pulse. Transistors suitable for these circuits must therefore tolerate high collector leakage capacitances (e.g. Type OC 23 with $N_C = 3$ W). In order to block the transistor in the rest position in spite of the positive emitter bias, diode D is needed in addition; this keeps the emitter voltage at the diode residual voltage.

4.4.3.3 Storage effect

To attain the necessary flank steepness of the collector current, the driving transistors must be over-controlled as a rule. This means that the storage effect, growing with increasing base current, can put in an unwelcome disturbing appearance.

As was mentioned earlier, the switch current must last for at least as long

as the switching time of the storage cores, i.e. the pulse duration corresponds as a rule to about 3 to 5 times the rise time. A longer pulse duration has no effect on the process of reversal of magnetisation; nevertheless it reduces the working speed of the store and raises the leakage capacitance of the drive transistor. Bearing these points in mind, the relatively large spread in storage effect from one transistor to another can be disturbing. With rapidly operating core stores we must therefore take extra measures to reduce the storage effect. According to relation (3.16)

$$\tau_s \sim \ln \frac{I_{BY} - I_{BX}'}{I_{BY} - I_{BX}}$$

the base blocking current I_{BY} must be increased to balance the harmful influence of the large control current I_{BX}' .

Fig. 4.78 shows an example of this [88]. The drive transistor T_2 is opened by a pre-amplification stage T_1 . T_1 is conducting in the resting position. The control signal blocks T_1 ; its collector voltage drops to the feed voltage V_{bat} and opens transistor T_2 . The base current rapidly decreases because of the voltage division via R and L . The circuit is so designed that T_2 is adequately controlled for the duration of the pulse. If T_1 is again opened, its collector voltage falls to the residual voltage and a comparatively strong positive current next flows from L into the base of T_2 . This quickly breaks down the excess charge in the base region. In practice the storage effect can thus be reduced to one fifth.

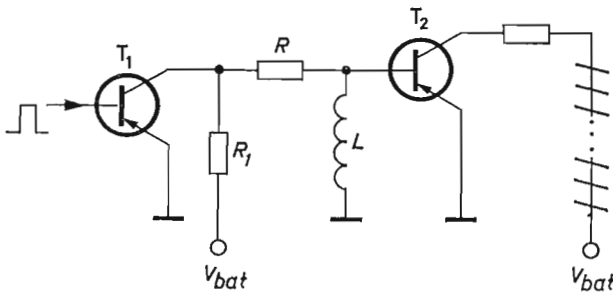


Fig. 4.78 Reducing the storage time by an inductance at the base

A similar result is also achieved by coupling the control pulses via a transformer, as Fig. 4.79 shows. The input pulse is differentiated; the rear edge supplies the required positive pulse which greatly reduces the storage time [87].

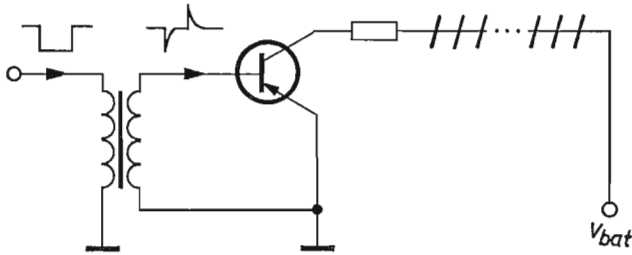


Fig. 4.79 Reducing the storage time by inductive coupling at the base

4.4.4 CORE STORE WITH TRANSISTOR WRITING AND READING CIRCUITS [89]

We shall describe a matrix store composed of four matrices each with 12×13 cores which can serve for the storing of 12 thirteen-place decimal numbers coded in binary tetrads. The storage capacity thus amounts to 624 bits. Thirteen pulses are needed for reading one decimal figure. The clock frequency amounts to 100 kc/s so that we get $130 \mu\text{s}$ for the access time of one figure.

The store is specifically for use in computers which operate in the decimal system.

Construction and method of operation:

The store is distinguished in several respects from the simple arrangement described in Section 2.6.4.2 (Fig. 2.27). Firstly, as well as the reading wire, each matrix includes a further line running through all the columns in the same direction, the blocking wire B which, in combination with a suitable working method, permits the stored information to be read without being cleared. Two further wires run through each line and column. In this way the writing and reading pulses can be sent in opposite directions through the cores; we can thus manage with pulses of one polarity, an essential requirement of the driving circuits. Finally, binary counters, the registers I and II (see Fig. 4.81) are used for the selection of the lines and columns. Suitable coding circuits ensure that the selection of the lines or columns occurs consecutively.

The four matrices stand one behind the other, as shown in Fig. 4.80. The storing of the four binary places of the tetrad of each decimal figure takes place one after another in the x direction, the storing of the digits of one single decimal number in the y direction, and that of different decimal numbers in the z direction. The line and column wires in the four matrices are con-

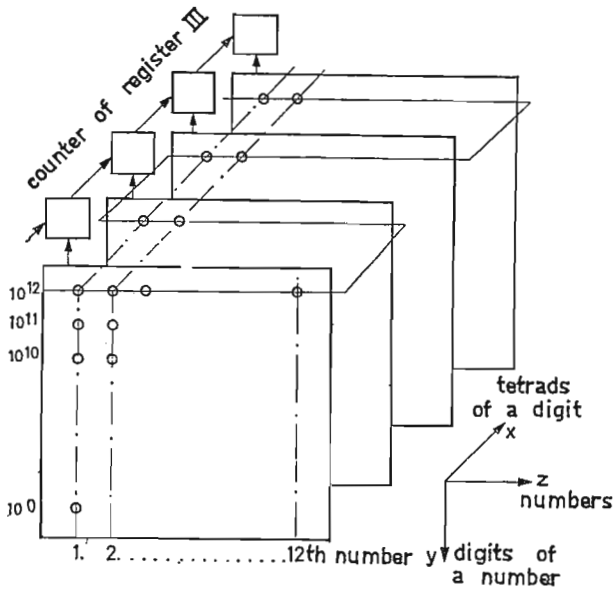


Fig. 4.80 Space arrangement of the four matrices for storing 12 thirteen-place decimal numbers

nected in series. Reading and blocking wires are taken out separately in each matrix. Each reading wire goes to a bistable element; these are connected to a decimal counter with tetrad coding (register III) which, in turn, is part of a counter store (see Section 2.6.2).

The construction of a matrix with the appropriate feed and selection circuits of the complete store is shown in Fig. 4.81. As well as the double line and column wires, the reading and blocking wires go through each core. The reading wire is led through the matrix according to the points explained in Section 3.5.6, while the blocking wire here is led back between the columns so that it runs through the next column again in the same direction

The registers I and II serve as line and column selectors. Here we are dealing with binary counters (see Section 2.4.3.1) which are brought into position "x" by x input pulses. The stages of register I are so back-coupled that the counter returns to the original position through the twelfth pulse, while register II is brought into the original position through the thirteenth pulse. The outputs of each bistable element feed the And-gates A_{1z} and A_{1s} constructed with diodes, which will be discussed later. These gates then pass the reading pulse A or the writing pulse D only for the chosen line and column. The output voltages of the line and column gates feed driving stages

which supply the necessary current amplitudes $I_m/2$ for the line and column wires. All the driving stages give pulses in the same direction. However, while the stages released by the A-pulse send the pulse through the matrix from left to right or from below to above, the pulses released by the D-pulses run from right to left and from above to below because of the opposite connection to the line and column wires. The A- and D-pulses thus produce

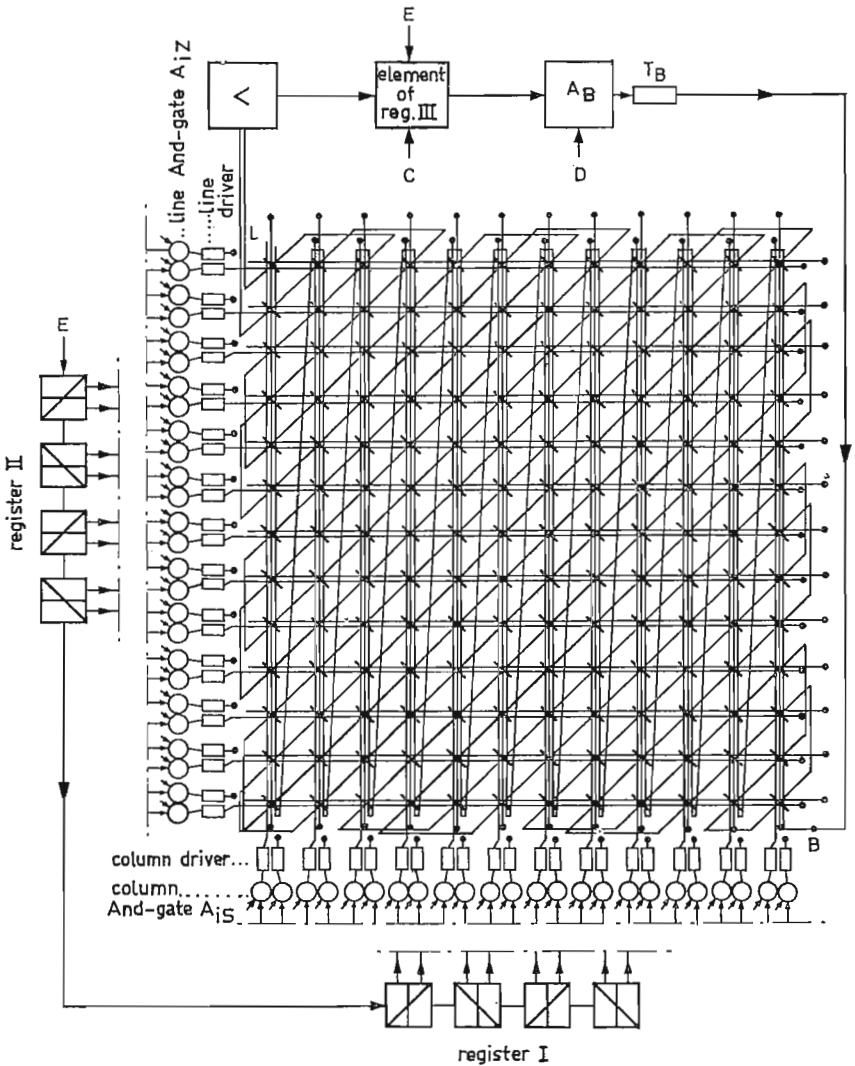


Fig. 4.81 Matrix with the writing and reading circuits

magnetisation in the opposite direction each time. Register III is made up of four bistable elements which are operated through the pulses in the reading wires of the four matrices after suitable amplification. The coding in the counter corresponds to the tetrad coding of single decimal digits.

The information of the cores is cleared when the store is read. It is stored, however, in register III so that it can be immediately re-written from here. The digit in register III can be read as often as desired through each ten C pulses (see Section 2.6.2). Register III serves also as receiver for the entry of fresh information.

We therefore have to distinguish three processes in the working method of the store: Reading the stored information, re-writing the information read and writing new information. The number and the temporary position of the individual pulses required to read and re-write a decimal digit are shown in Fig. 4.82. Because of the series connections of the corresponding line and column wires of the four matrices, a complete tetrad and thus a decimal figure, is taken up simultaneously each time.

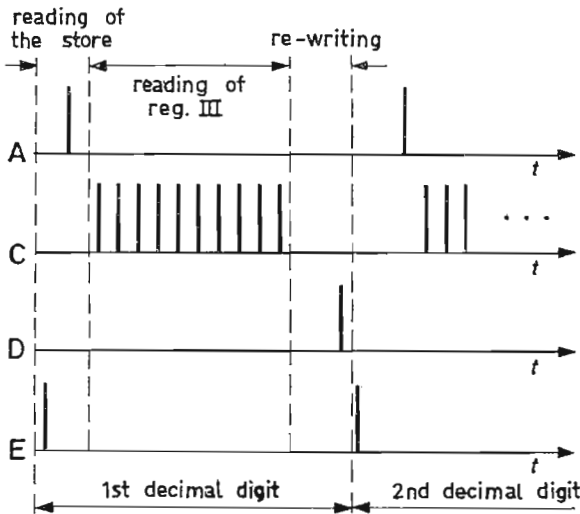


Fig. 4.82 Number and momentary position of pulses during reading and re-writing of a decimal digit

The *reading* of the individual digits of a stored decimal number proceeds in the following way: Register III is in the 0 position. Registers I and II should be in position "1" through which the pair of gates for the first line and column will be opened. The selection of elements K_{11} of the four matrices

results from this. Now the first gates of all pairs each receive an A-pulse which, however, can only release a pulse $I_m/2$ in the first line and first column. Through the coincidence in core K_{11} of each matrix, a magnetisation occurs in the direction of the negative remanence. If a core contains an "L", it triggers over and a pulse is induced in the reading wire of the corresponding matrix which after amplification brings the corresponding bistable element of register III into the "L" position. (If the core were in condition "0", the small disturbing pulse in the reading wire would not be able to affect register III.) The first digit of the first number is now in register III. It is here passed on to the next required place through ten C pulses so that the digit is retained in register III to be again re-written into the store.

The *re-writing* of the read digit in register III takes place in the following way: One D-pulse is transmitted to each second gate which produces $I_m/2$ pulses of opposite effect (reversed course) in the same line and column previously chosen at the reading. These would bring into position "L" each core K_{11} which is in position "0" after the reading. At the same time, however, this D-pulse is conveyed to the gates A_B of each matrix which are controlled by the corresponding bistable element of the counter in register III. These gates are then only opened if the corresponding flip-flop is in position "0". Then the D-pulse can send a pulse $I_m/2$ over the driving stage T_B into the blocking wire which, in the chosen core, reduces the two $I_m/2$ pulses in the line and column wire to one $I_m/2$ pulse because of the contrary course of direction; this core, K_{11} , remains in condition "0". If, on the other hand, an "L" is in the corresponding element of register III, A_B then remains blocked; the selected core is brought into the "L" position through the two $I_m/2$ pulses in the line and column wires.

In this way the original information is again stored in the core. The choice of the next line now takes place through an E-pulse which arrives simultaneously at each element of register III and here triggers back to "0" all the elements in position "L". The next A-pulse reads cores K_{21} and thus the second digit of the first number, and so on. After 13 such cycles in all, the first column has been read. With the next E-pulse, register II triggers back to its initial position; the resulting output pulse brings register I into position "2" so that with 13 further cycles the second column can be read. The whole store is interrogated after 12 times 13 cycles altogether.

With the *entry* of a new digit into the store, the digit is first brought into register III. An A-pulse then puts into the 0 position the cores selected through registers I and II (in the same way as for the reading), whereby the reading winding must be switched off so as not to affect the register. Exactly as with the re-writing, a D-pulse triggers the core into the "L" position if

there is no "0" in the corresponding element of register III to block the reversal of magnetisation via gate A_B . An E-pulse then triggers register III into the 0 position for the reception of the next digit.

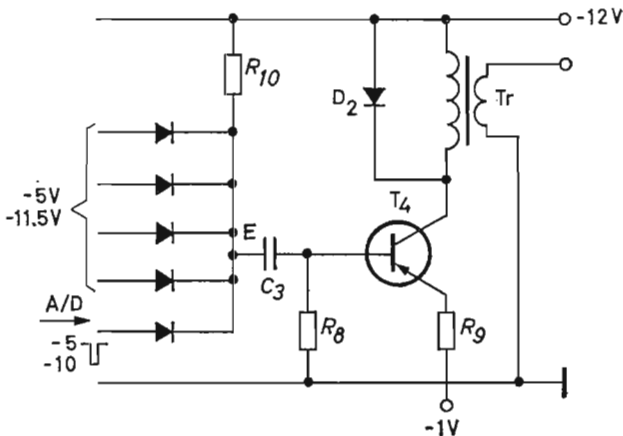
Core materials:

The cores used are of the substance 6 D 3 (see Table 3.6). For optimum ratios (at 40 °C) the switch current should be 2×350 mA (see Fig. 3.30), the pulse duration about 2 μ s and the rise time 0.2 μ s. The amplitude can fluctuate by $\pm 10\%$.

The And-gates

Fig. 4.83 shows the circuit diagram of the diode gates used. The first four inputs are connected to one or the other input (-5 and -11.5 V) of the bistable elements of registers I and II. This is done in such a way that each counter position supplies one And-statement for the selected line or column. The (negative) A or D pulses whose level lies between -5 and -10 V are applied at the fifth input. A pulse at the fifth input can only pass through the gate when all the other inputs are at -11.5 V.

Since the gate cannot be loaded, a transistor is connected into the emitter circuit as separator stage, counter-coupled through the resistance R_9 . The coupling is capacitive. To suppress the influence of small input disturbing



T_4 ... OC 44

D_2 ... OA 95

Tr ... Shell core 14/8-00-3E,
120/24 Wdgs.

$C_3 = 10$ nF

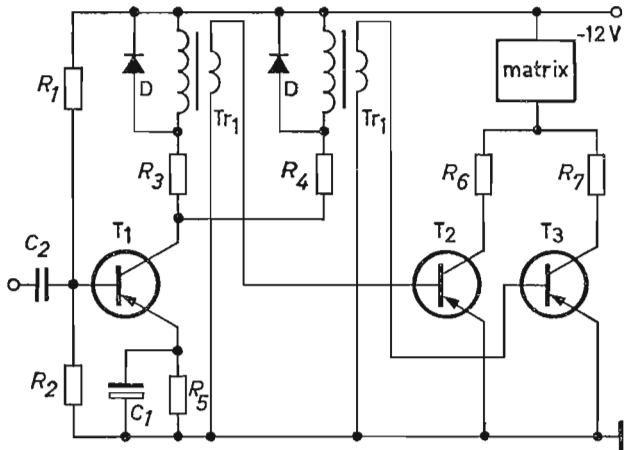
$R_8 = 100$ k Ω }
 $R_9 = 100$ k Ω } $\pm 5\%$, $1/3$ W

Fig. 4.83 Circuit of an And-gate (with separator stage)

voltages, the emitter is biased at -1 V. The voltage at the base thus lies, in the absence of input voltage, at about $+1$ V and, with input voltage present at about -5 V. At the collector, and thus at the primary winding of the transformer, the voltage alters by 7 V (between -12 V and -5 V). T_r serves as a resistance transformer for the low-resistance input of the driving stages. Diode D_2 should suppress the overswing of the voltage at the transformer when the transistor is switched off.

The driving stages:

Fig. 4.84 shows the circuit of a driving stage. Transistor T_1 is conducting in the rest condition through the voltage divider R_1/R_2 so that the current through the primary windings of each of the transformers T_{r1} amounts to about 10 mA.



R_1	$= 15 \text{ k}\Omega$				
R_2	$= 5 \text{ k}\Omega$	$\pm 5\%$, $1/3 \text{ W}$	R_5	$= 120 \Omega$	
R_3, R_4	$= 820 \Omega$		R_6, R_7	$= 66 \Omega$	$\pm 10\%$, $1/2 \text{ W}$
T_2, T_3	\dots OC 44				
D_1, D_2	\dots OA 95				
T_{r1}	\dots Shell core S 14/8-00-4B,				
	210/24 Wdgs.				
				$C_1 = 8 \mu\text{F}$	25 V
				$C_2 = 10 \text{ nF}$	

4.84 Circuit of a driving stage

The resistances R_3 and R_4 reduce the collector voltage so as to keep the collector leakage capacitance sufficiently low. The collector resistance R_5 is shorted by C_1 , producing a comparatively low value of input resistance. On the other hand, a small positive input pulse from the And-gate is then enough to block transistor T_1 . Through the secondary voltage (see Fig. 4.85) of the transformers, transistors T_2 and T_3 are then controlled to saturation point.

To maintain the necessary amplitude of 350 mA, two transistors are wired in parallel. The base currents (see Fig. 4.85b) must here be large enough for the collector current (Fig. 4.85c) to have the necessary rise time of 0.2 μ s.

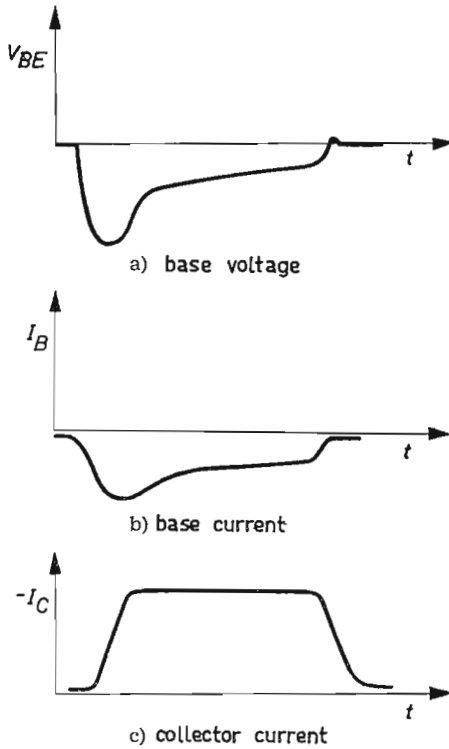


Fig. 4.85 Currents and voltages of the driving transistors T_2 and T_3

The driving stages are released by an A or D pulse. Since one cycle comprises 13 pulses (see Fig. 4.82), the maximum working frequency of the driving stages is about 8 kc/s with a clock frequency of 100 kc/s. In this way the mean leakage capacitance of the transistors is low in spite of the high pulse loads.

The reading amplifier:

This has the task of triggering the corresponding bistable multivibrator of register III by means of the output pulse induced at the reading of an L. The disturbing pulse produced at reading, on the other hand, must not influence register III. Here we can differentiate between

a) the total disturbing voltage in the reading wire at the reading of an "L",

resulting from stimulation with $-I_m/2$ of the cores in the chosen line and column, the cores which contain an "L" contributing more than those in the "0" condition,
and

- b) the disturbing voltage at reading an "0".

Furthermore, the amplifier should not respond to the voltages in the reading wire produced during writing.

Fig. 4.86 shows the output voltage at the reading wire when a core in a matrix is read. The voltage portion during t_a corresponds to the uncompensated remainder of the rapid induction voltages in the cores supplied with $-I_m/2$. The unbroken curve drawn in the interval t_b gives the input voltage of the selected core at the reading of an "L", the dotted curve that at the reading of an "0". Finally, the voltage in interval t_c results from the return of the core to the remanence after cessation of the stimulus.

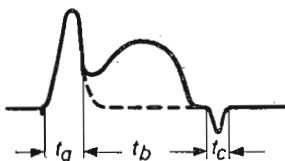


Fig. 4.86 Output voltage at the reading wire

In the store concerned, the reading wire is led diagonally through the matrix to reduce the disturbing pulses, i.e. the polarity of the output voltages changes from core to core. The suppression of the output voltage induced at writing (which has the opposite direction to that during reading) can therefore not occur with a reading amplifier only responding to one polarity. Other methods must be used here to ensure that the amplifier is only gated during the reading.

As we also observe from Fig. 4.86, the portions t_a and t_b of the output voltage can no longer be separated in respect to amplitude if the disturbing voltage reaches the same dimensions as the effective voltage in interval t_b , as would be the case with a larger matrix. Here we have to rely on the aid of the periodic selection so that we only switch the amplifier in for period t_b . This can be done with the reading circuit shown in the block diagram of Fig. 4.87. The amplifier takes up the whole output voltage and, independent of the polarity of the input voltage, always delivers a negative output pulse. This feeds an And-gate which is opened via the other inputs d and e through appropriate pulses only for the period t_b at the reading. Fig. 4.88 shows the

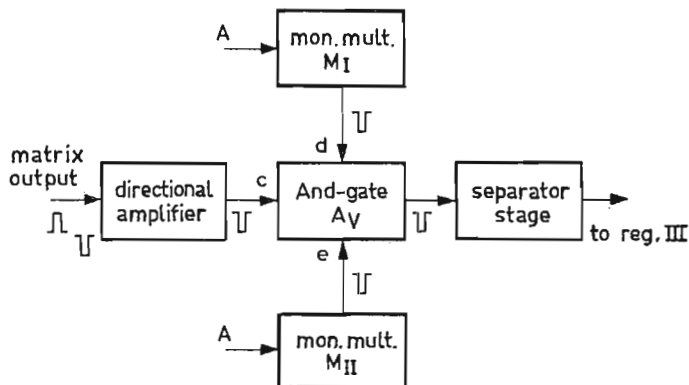


Fig. 4.87 Block diagram of the reading amplifier

three input voltages and the output voltage of the gate A_V . It is opened by negative input voltages above 5 V. Pulse I has the duration t_a , pulse II the width $t_a + t_b$. The gate passes the voltage from the amplifier only in the overlapping range t_b of the two inputs d and e , that is to say the voltage values which lie between -5 and -10 V.

The two pulses I and II are produced by monostable multivibrators which are released in each case by the A-pulse (see Fig. 4.82). The output of multivibrator I in the rest condition lies at -10 V, and after release delivers a positive pulse of 5 V and duration t_a . Multivibrator II is in the resting con-

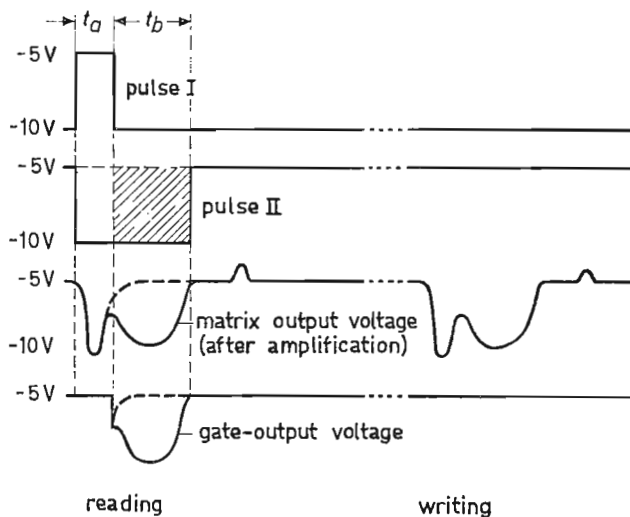


Fig. 4.88 Voltages at the gate A

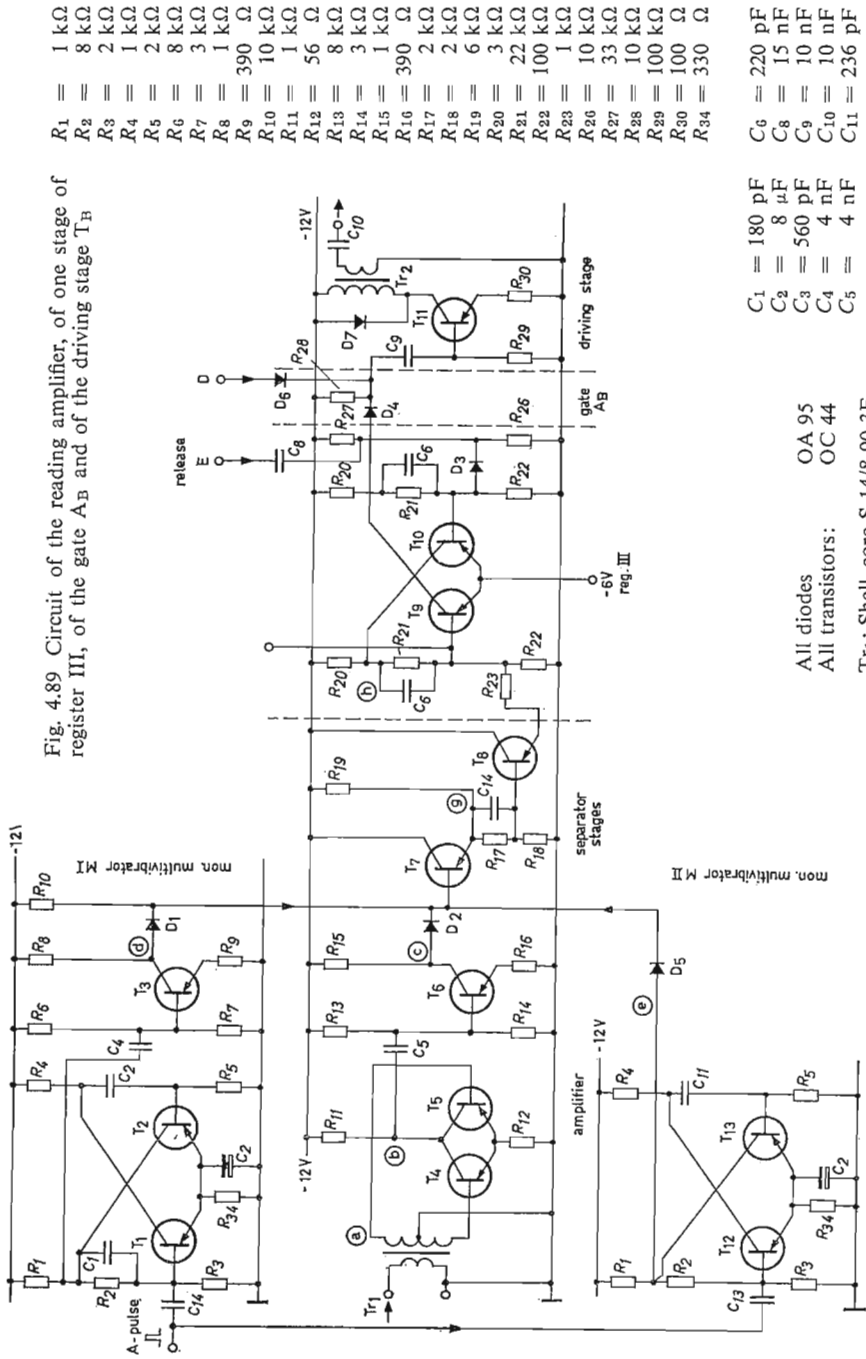


Fig. 4.89 Circuit of the reading amplifier, of one stage of register III, of the gate AB and of the driving stage T_H

- R₁ = 1 kΩ
- R₂ = 8 kΩ
- R₃ = 2 kΩ
- R₄ = 1 kΩ
- R₅ = 2 kΩ
- R₆ = 8 kΩ
- R₇ = 3 kΩ
- R₈ = 1 kΩ
- R₉ = 390 Ω
- R₁₀ = 10 kΩ
- R₁₁ = 1 kΩ
- R₁₂ = 56 Ω
- R₁₃ = 8 kΩ
- R₁₄ = 3 kΩ
- R₁₅ = 1 kΩ
- R₁₆ = 390 Ω
- R₁₇ = 2 kΩ
- R₁₈ = 2 kΩ
- R₁₉ = 6 kΩ
- R₂₀ = 3 kΩ
- R₂₁ = 22 kΩ
- R₂₂ = 100 kΩ
- R₂₃ = 1 kΩ
- R₂₄ = 10 kΩ
- R₂₅ = 33 kΩ
- R₂₆ = 10 kΩ
- R₂₇ = 33 kΩ
- R₂₈ = 10 kΩ
- R₂₉ = 100 kΩ
- R₃₀ = 100 Ω
- R₃₁ = 330 Ω

- C₆ = 220 pF
- C₈ = 15 nF
- C₉ = 10 nF
- C₁₀ = 10 nF
- C₁₁ = 236 pF

- C₁ = 180 pF
- C₂ = 8 μF
- C₃ = 560 pF
- C₄ = 4 nF
- C₅ = 4 nF

All diodes OA 95

All transistors: OC 44

T₁: Shell core S 14/8-00-3E,
180/180/18 Wdgs.

dition at -5 V and after release through the A-pulse yields a negative pulse of 5 V and duration t_b . The gate itself is again constructed with diodes and requires a separator stage (since it cannot be loaded) which then feeds register III.

The circuit of the amplifier, the monostable multivibrators, the And-gates A_V and the separator stage is shown in Fig. 4.89, together with a stage of register III, the And-gate A_B and the driving stage I_B for the blocking pulse. The reading pulse arrives at the carrier T_1 which feeds the base of transistors T_4 and T_5 . These are counter-coupled through the emitter resistance R_{12} so that the input resistance of the opened transistor is approximately

$$r_i \approx (1 + a_e) \times (R_{12} + r_e)$$

With $a_e \approx 50$ and $r_e = 25 \Omega$ (emitter-diode resistance) we find that $r_i \approx 4 \text{ k}\Omega$. The carrier needs a translation ratio of 10 so that transistors T_4 or T_5 are controlled. The reading wire is thus loaded with 40Ω . With the small matrix used here the internal resistance of the reading wire is so low that this input resistance does not charge the matrix to any extent. The two transistors T_4 and T_5 are blocked in the rest condition. According to the polarity of the output pulse at the reading wire, one of the two transistors is opened through the negative pulse from one of the secondary windings of the transformer.

The And-gate consists of the three diodes D_1 , D_2 and D_3 . The input c lies without signal voltage at -5 V. Only when the two other inputs d and e are more negative can a negative reading pulse at the separator stage control the base of T_1 via the diode D_2 .

The two monostable multivibrators are made up of the transistors T_1 and T_2 , or T_{12} and T_{13} . Transistor T_3 serves to change the polarity of the pulse. With transistor T_7 operating in the collector circuit, the emitter is negatively biased with the aid of resistance R_{19} , so as to suppress disturbing pulses produced at the reading of an "0". On the other hand, the biased emitter of T_7 does not permit the direct release of the multivibrator in register III. For this reason a further transistor T_8 , working in the collector circuit, must be intermediately connected.

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